MICROFLUIDIC THERMAL MANAGEMENT OF 2.5D AND 3D MICROSYSTEMS

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MICROFLUIDIC THERMAL MANAGEMENT OF 2.5D AND 3D MICROSYSTEMS

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LIST OF SYMBOLS AND ABBREVIATIONS

a_i	Coefficient of the polynomial.
$\hat{a}$	Matrix with all a_i.
A_c	Heat transfer areas between coolant and silicon surfaces, m^2.
A_{chip}	Chip area, cm^2.
Cp	Specific heat at constant pressure, J/kg/K.
D_{lg}	Longitudinal diameter, μm.
D_{pin}	Pin diameter, μm.
D_{tr}	Transverse diameter, μm.
f	Friction coefficient.
FP	Fin thickness, μm.
FT	Fin thickness, μm.
g	Acceleration due to gravity, m/s^2.
H_{pin}	Height of pin, μm.
H_{rise}	Height difference between condenser and evaporator, μm.
h	Heat transfer coefficient, W/m^2k.
h_{amb}	Ambient heat transfer coefficient, W/m^2k.
h_{hts}	Heatsink heat transfer coefficient, W/m^2k.
k_l	Thermal conductivity of liquid, W/m K.
k_{si}	Thermal conductivity of silicon, W/m K.
L_c	Chip length, cm.
$\dot{m}$	Mass-flow rate, kg/s.
Nu	Nusselt number.
P	Chip power density, W/cm^2.

ΔP	Pressure drop, kpa.
P_b	Power density of background heater, W/cm^2.
P_{hs}	Power density of hotspot, W/cm^2.
P_l	Localized power provided for each heater, W/cm^2.
q''	Heat flux, W/cm^2.
Q	Flow rate, L/hr.
q_{conv}	Conduction heat flux, W/cm^2.
q_{gen}	Generated heat, W/cm^2.
q_{pin}	Conduction through pin, W/cm^2.
R	Resistance, Ω.
Re	Reynolds number.
S	Fin pitch, μm.
S_{lg}	Longitudinal pitch, μm.
S_{tr}	Transverse pitch, μm.
t	Time, s.
T	Temperature, ºC.
T_{amb}	Ambient temperature, ºC.
T_{FPGA}	Temperature of FPGA, ºC.
T_{in}	Coolant inlet temperatures, ºC.
T_{ini}	Initial temperature, ºC.
T_{out}	Coolant outlet temperatures, ºC.
T_s	Chip surface temperatures, ºC.
T_{tra}	Temperature of transceiver, ºC.
u	Velocity component in x-direction, m/s.

v	Velocity component in y-direction, m/s.
V	Voltage, V.
w	Velocity component in z-direction, m/s.
W	Chip width, cm.
$\hat{x}$	Matrix $\hat{x}$ with all x.
$\hat{x}'$	Transpose of matrix $\hat{x}$.
x_i	Level of factor i.
x_j	Level of factor i.
X	X axis of the fixed XYZ co-ordinate.
$\hat{y}$	Matrix $\hat{y}$ with all y.
Y	X axis of the fixed XYZ co-ordinate.
Z	X axis of the fixed XYZ co-ordinate.
ρ	Mass density, kg/m^3.
μ	Coefficient of dynamic viscosity, $Ns=m^2$.
δ	Thickness, μm.

SUMMARY

Both 2.5 dimensional (2.5D) and 3 dimensional (3D) stacked integrated chip (SIC) heterogeneous architectures are promising to go beyond Moore's law for compact, high-performance, energy-efficient microsystems. However, these systems face significant thermal management challenges due to the increased volumetric heat generation rates, and reduced surface area. In addition, highly spatially and temporally non-uniform heat generation occurs due to different functionalities of various heterogeneous chips. This dissertation focuses on thermal management challenges for both 2.5D and 3D-SICs, by utilizing micro-gap liquid cooling with enhanced non-uniform heterogeneous pin-fin structures. Single phase convection thermal performance of heterogeneous pin-fin enhanced micro-gap liquid cooling under non-uniform power map has been evaluated under steady state conditions. Heat transfer and pressure drop characteristics of dielectric coolants in cooling manifold with cooling enhanced structure and hergeneous pin-fins have been parametrically studied by full-scale computational fluid mechanics/heat transfer (CFD/HT) to achieve non-uniform cooling capacities for multi-chip test structures of 2.5D-SICs. Non-uniform heterogeneous pin-fin structures in cold plates have been numerically and systematically optimized using design of experiment method, coupling with full-scale CFD/HT simulations. A compact thermal model accounting for both spatially and temporally varying heat-flux distributions for inter-layer liquid cooling of 3D-SICs, with realistic leakage power simulation feature has also been developed as a thermal-electrical co-design tool for 3D-SICs. In addition to the active micro-gap liquid cooling thermal managements, this dissertation also investigates the passive micro-gap two-phase liquid

cooling using a miniature-thermosyphon with dielectric coolant Novec 7200, for future 3D-SICs. Experimental characterizations, including heat transfer measurements, and bubble flow visualizations are performed under two phase conditions. Implementation of miniature-thermosyphon on 3D-SICs provides non-uniform in-plane as well as cross-plane cooling capacities, which can be used and further enhanced for 3D-SICs thermal management with heterogeneous chips.

CHAPTER 1. INTRODUCTION

1.1 2.5D and 3D-SIC with TSV

"More-than-Moore", making products by integrating multiple heterogeneous technologies into one minimized integrated electronic system, successfully emerged around the middle of the previous decade [1]. Almost every single cellphone, and handheld, and wearable devices are realized by integrating heterogeneous technologies, including logic, memory, various sensors, radio frequency (RF), and micro-electro-mechanical systems (MEMS). "More-than-Moore" contributes to overcoming the limitation of system scaling, and enabling mobile devices with diverse and complicated functions.

Accompanying this revolution, high-speed and high-quality data transfer within and between every mobile device are inevitably required. Recent data show that there was a greater than 10 time increment in the mobile data traffic from 2012 to 2017, and the daily data traffic in 2017 approached quintillion bytes [2-3]. Handling such data traffic is a huge challenge for semiconductor manufacturing and packaging industries, and requires

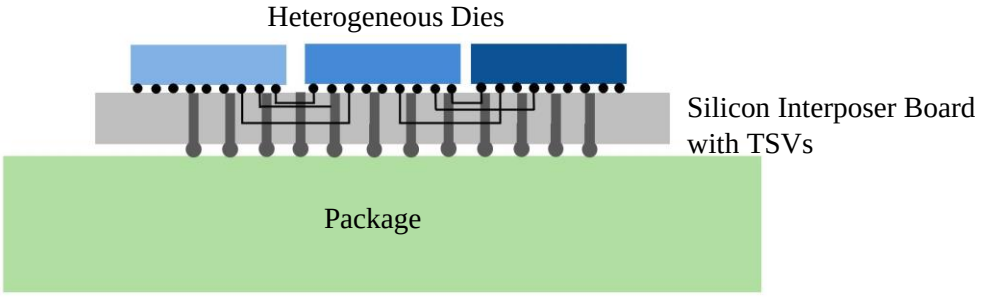


Figure 1 : Illustration of 2.5D-SICs.

advances in current silicon technology platforms to transfer large amounts of data rapidly and accurately with lower power consumption.

In traditional 2D-ICs, 16nm and transistor gates have been accomplished as fin field-effect transistors (FinFet) which are widely invested and have contributed to scaling since 2001 [4]. However, physical limitation of atom layer thickness still exists, which explains the prediction that transistor size will still decrease with time but eventually remain constant [5-7]. In addition to the scaling problem of transistors, interconnects of transistors have become a major bottleneck for high-performance computing systems [8]. As ICs contain more electronic components in planar direction, the interconnects of these components become longer, which increases both latency and required switching energy. Higher energy consumption from the longer interconnection length contributes to intensifying heat generation because of Joule heating. Thus, these factors contribute to increases in latency and consumption, and reductions in the expected benefits from scaling.

However, both 2.5D and 3D stacked ICs (SICs) with through-silicon-vias (TSVs) [9-11], are promising solutions to the Internet of everything (IOE) challenges. A cross-section of a 2.5D-SIC is illustrated in Fig. 1 (a) [12]. In this example, three conventional chips (logic, CMOS, and DRAM) are stacked with micro-bumps onto a base layer of silicon interposer. Instead of having active circuitry, the interposer only contains interconnects: horizontal ones between different dies through multiple metal layers of interposer, and vertical ones through TSVs between dies and the package substrate toward the external world. Another application would be photonic integrated circuits (PIC) by implementing 2.5D-SICs technology [2], which has been shown in Fig. 2 (b). Not limited to mobile system feature enablement, PIC with 2.5D-SICs would be able to meet the performance

requirement of data-centers, super-computers, and high-performance-networking. Providing vertical interconnects, TSVs naturally lead to the design of 3D-SICs, which have several chips vertically stacked together. 3D-SICs could reduce the wire interconnection length by as much as 50% [13]. Hence, the shorter wire length reduces the global resistive-capacitive delay and increases the wire-limited clock frequency by 3.9 times [14]. Thus, remarkable power reduction in the interconnection can be expected. In addition, 3D structures also achieve wide bandwidth buses between functional blocks in the chips [15], this could contribute to improved signal quality [16-18]. Fig. 2 (a) presents an illustration of a future 3D-SICs system [18]. The potential benefits of 3D-SICs include multi-functionality, increased performance, increased data bandwidth, increased yield and reliability, flexible heterogeneous integration, and reduced overall costs. Compared to 2.5D-SICs, 3D-SICs have additional benefits: a small footprint and form factor, which are crucial for many small, portable, and wireless applications.

In the future, 2.5D-SICs and 3D-SICs hybrid combinations can be expected as: hybrid systems containing multi-die 3D stacks on top of a base of 2.5D-SICs silicon interposer [2]. Both 2.5D and 3D-SICs have thermal management challenges because of the increasing power dissipation of heterogeneous dies and limited system space. A review of the literature on thermal management related to these technologies is presented next.

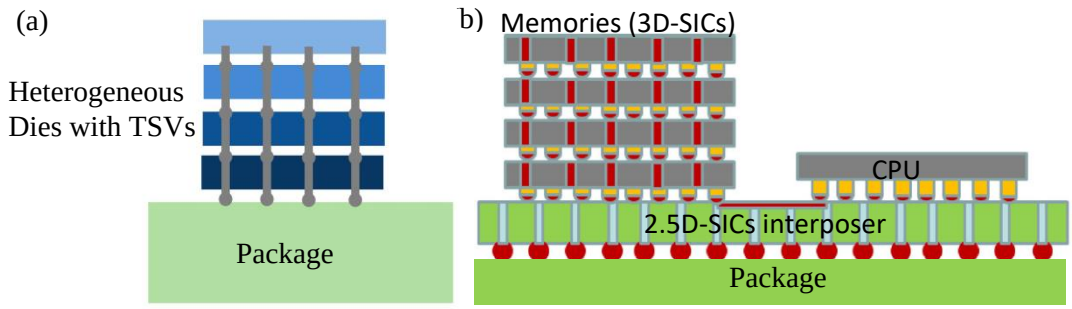


Figure 2: (a) Illustration of future heterogeneous 3D-SICs. (b) Schematic of 2.5D-SICs and 3D-SICs hybrid combinations [2].

1.2 Thermal Management Methods for 2.5D and 3D-SICs

Both 2.5D-ICs and 3D-ICs have hotspot thermal management challenges because of their compact structures and various heat fluxes generated from heterogeneous chips. These thermal characteristics with limited spaces contribute to the requirements of higher cooling capacity, which are mainly provided by liquid cooling.

1.2.1 Active Cooling Studies for 2.5D-SICs

2.5D-SICs with closely placed heterogeneous die are considered to be a first step towards full 3D integration. Hisada and Yamada [19] studied thermal performance of silicon interposer flip chip plastic ball grid array (FCPBGA), glass interposer FCPBGA, and conventional multi-chip module (MCM) FCPBGA, assuming that a high-power logic chip and a low power memory chip are packaged in each package configuration. CFD/HT was used to analyze thermal performance of each package with the variation of heat dissipation configuration: lidless, lidded and heat sink attached on lid. The effects of airflow rate and power consumption of logic chip were also analyzed. Logic and memory chips of size 15 mm × 15 mm, and 10 mm × 7 mm, respectively, were mounted on an

organic build-up substrate. Power consumption of the memory chip was 1 W, and logic chip varied from 5 to 80 W. The ambient temperature was set at 20 °C. The variations of linear airflow were 0.5 to 3.0 m/s. Heat dissipation from the heat sink is dominant, and heat dissipation from the substrate to the board is negligible in this case.

Zhang et al. [20] investigated thermal characteristics of 2.5D packages in both bare-die package and over molded package. The test vehicle with 18 mm × 18 mm × 0.1 mm interposer had three chips, two of which were dummy chips, and the third was a 5 mm × 5 mm thermal test die (0.3–2.45 W). Thermal resistances were measured from junction to the ambient, from junction to the board, and from junction to top casing. Khan et al. [21] investigated a 2.5D/3D stacked package with silicon interposers to integrate a processor (8.5 mm × 8.5 mm × 0.1 mm) dissipating 20 W, and two memory chips (4.5 mm × 4.5 mm × 0.1 mm) dissipating 0.5 W each. The package design was optimized for structural and thermal performance. Thermal enhancement techniques like thermal via and thermal bridging were analyzed, and the package design was found suitable for a 3 W power by natural convection cooling. The package thermal performance was further improved by designing a silicon heat spreader. The 3D package with silicon heat spreader was suitable for dissipating 20 W power with an external air-cooled heat sink.

1.2.2 Active Liquid Cooling Studies for 3D-SICs

For a 3D-SICs package, the external cooling capacity of the stacked chips is limited, due to the reduced surface area. Additionally, the interior tiers in the 3D stack can have significant temperature gradients. In the recent decade, many studies have focused on

forced convection interlayer liquid cooling, which could reduce the thermal resistance and have higher cooling performance, compared to air cooling.

Mizunuma et al. [22] presented a fast and accurate thermal-wake aware compact thermal model for integrated micro-gap 3D-SICs. The temperature of the liquid near the solids exceeded the mixed mean liquid temperature by a large amount. As the liquid flows downstream, the thermal energy diffuses in all directions, and produces exponential decay of the downstream temperature field. This phenomenon is referred as thermal-wakes [23-25]. Alfieri et al. [26] used a porous medium method with variable properties to model the heat transfer in 3D-SICs. The cooling layers with an array of in-line cylindrical pins were replaced by ultra-thin porous medium layers with orthotropic thermal conductivity, and temperature dependent material properties. The correlations for the heat transfer coefficient and pressure drop required for non-equilibrium porous medium simulations were obtained from separate 3D conjugate heat transfer simulations on 20 inline pins under realistic boundary conditions. Kearney et al. [27] investigated microfluidic cooling driven by an integrated AC electro-kinetic pump embedded in the gap walls. This cooling method did not reduce the global temperature of a 3D IC architecture, but it contributed to making the temperature distribution within the 3D IC more uniform.

Arvind et al. [28] proposed a compact transient thermal model (CTTM), called 3D ICE, for the thermal simulation of 3D ICs with multiple inter-tier micro-gap liquid cooling. The authors claimed that their approach should be accurate when the cell dimension is less than few hundred micrometers. This compact thermal model provides rapid predictions, because it does not compute the thermal wake function, which increases the computation time, every time when the flow condition or gap dimension are changed. Without the need

for numerical pre-simulation, the 3D ICE model allows for the incorporation of any reliable correlation based on the heat transfer coefficient. The authors also built a 3D-IC model based on modeling the fluidic layer as a porous medium to solve the inline and staggered pin fin configurations [29]. The model is compatible with thermal CAD tools for ICs, and offers high speed-up over commercial CFD simulators. In addition, the model is flexible and provides a generic framework in which heat transfer coefficient data from numerical simulations or existing correlations can be incorporated, depending upon the speed/accuracy needs of the designer. However, the heat transfer coefficient correlations in approach are only functions of the Darcy velocity. They do not reflect the effects of pin fin dimensions, including the diameter, height, transversal, and longitudinal spacing, on the heat transfer coefficient. The thermal and hydraulic characteristics of different dimensions are not expected to be the same.

Wan et al. [30-31] established a new correlation of the friction factor and Colburn j factor for dense arrays of micro-pins (parametric runs over 22< Re <357, pitch/ diameter ratios of 1.5 to 2.25, and height/ diameter ratios of 1.5 to 2.25), based on CFD/HT modeling. The thermal characteristics under liquid cooling were investigated using a compact thermal model. The model first discretized the physical space into control volumes, each around a single pin. Energy balance equations were built for each control volume. A detailed analysis of fin energy flow was also included. Four alternative packaging organizations were studied and compared, based on the architecture of a 16 core, x 86 multicore die stacked with a second die hosting an L2 SRAM cache. Simulation results of four packaging organization were compared, and the optimized packaging structure was an integration of two tiers and two pin fin enhanced micro-gaps with the high-power

dissipation tier at the top. This optimization could achieve significant energy saving, and reduction in leakage power. Serafy et al. [32] co-designed 3D-SICs architectures with four CPU layers and microfluidic heatsinks to simultaneously optimize the performance and cooling capacity. The article proved that the co-design approach with compact thermal simulation function achieves better performance and energy efficiency than optimizing only the cooling capacity or the vertical bandwidth.

1.2.3 Passive Liquid Cooling Studies for 2.5D and 3D-SICs

In contrast to the active micro-gap liquid cooling mentioned above, two-phase miniature-thermosyphon, a passive two-phase cooling method without mechanically rotating components like pump, has been used effectively in electronics cooling [33-34]. Without the concern of pump failure, such passive liquid cooling loop relies on the buoyancy driven fluid circulation due to the temperature gradient driven density differences. In contrast to regular size thermosyphon systems that are commonly applied in building solar heating systems, Miniature-thermosyphons with compact rising altitude for electronic cooling offer the promise of quiet, reliable, and low-cost operation.

Extensive studies have focused on the close loop thermosyphon cooling performance, including coolant properties, heat load, filling ratio, supplied cooling of the condenser, and altitude difference between condenser and evaporator from experimental and simulation perspectives. Pal et. al [35] presented a compact two-phase thermosyphon for a Pentium 4 microprocessor cooling in a commercial desktop computer HP Vectra VL800. Deionized water and PF5060 were selected as coolants, which were proven to affect the thermosyphon cooling performance significantly. The condenser was cooled by

air cooling which could limit the power input, ranging from 56 W to 80 W, into the evaporator. Evaporator orientation had limited effects on the thermosyphon performance. Khandekar et.al [36] investigated the overall thermal resistance of closed two-phase thermosyphon using nanofluidic coolant of 1% by weight of Al_2O_3, CuO and laponite clay. Compared to water coolant, nanofluidic thermosyphon had enhanced cooling performance. They also observed the wettability on copper substrate, and concluded that the increase in wettability and entrapment of nanoparticles in the grooves of the heat transfer surface would eventually contribute to poor thermal performance. Ong et. al [37] presented the thermal-hydraulic performance of a miniature-thermosyphon system with riser height of 15 cm. R134a was selected as a coolant, with filling ratios in the range of 67% to 83%. Multi-microchannel copper evaporator, mounted on top of a CPU emulator had uniform heat fluxes up to 61.4 W/cm^2 with mass flow rates up to 10 kg/hr. The miniature-thermosyphon loop was envisioned to be applicable to 2U height servers with cooling need up to 80 W/cm^2.

Haider et. al [38] presented a simulation model for a closed loop two-phase thermosyphon (CLTPT) involving co-current natural circulation. This model considered mass, momentum, and energy balances in the evaporator, rising tube, condenser, and the falling tube. Pressure drop of the two-phase flow was evaluated by a homogeneous two-phase flow model. Saturation temperature with thermodynamic constraints also depends upon the local heat transfer coefficient and the two-phase flow patterns inside the condenser. Chip temperature was simulated with boiling characteristics of the enhanced structure. Simulation results generally fit the experimental data with dielectric working

fluid PF-5060. It is worth noting that majority of modeling uncertainties come from local condensation heat transfer coefficient.

Marcinichen et. al [39] developed a steady-state simulation code to simulate steady state thermal performance of their thermosyphon loop. This code was verified by their experimental evaluation of their thermal-hydraulic performance with heat fluxes from 45 to 60 W/cm^2. Lamaison et. al [40] presented a transient dynamic simulator with a set of coupled partial differential equations (temporal and spatial) to simulate the micro-evaporator, riser, condenser, and down comer in the thermosyphon system. Simulations of temperature and system pressure with six different heat fluxes from 15.2 to 33.1 W/cm^2 are compared to experimental results with mean errors of 2.9 and 3.1%.

Although extensive studies mentioned above have studied the characteristics of miniature-thermosyphon thermal management via both simulations and experiments, none of them have implemented miniature-thermosyphon into 3D-SIC cooling. The cooling capacity of 3D-SIC thermosyphon for each layer of 3D-SICs remains unknown.

1.2.4 Pin-fin Enhanced Micro-Gap Liquid Cooling

Among the various passive cooling and active cooling methods with their advantages [36-37, 41-44], pin-fin-enhanced micro-gap liquid cooling, as one active cooling method, would potentially have enough cooling capacity for high-performance heterogeneous chips with 2.5D/3D-SIC structures.

Various studies have examined this cooling method from a number of perspectives. Peles et al. [45-46] investigated the heat transfer and pressure drop phenomena of heat

sinks with various fin structures. They tested the micro-pin-fin structure, which has a 1 cm × 1 cm base area with a staggered array of cylindrical fins. The hydraulic diameters of the fins range from 150 to 350 μm with a height of 400 μm. The ratio of pitch to diameter is 1.5. They implemented uniform power maps from 5 to 35 W/cm^2 and used water with a flow rate 3.2 mL/min as a coolant. This test entailed the use of cylindrical pin fins of circular cross-sections at uniform spacing for a uniform heat flux. Their experimental results proved that the pin fin-enhanced micro-gap has low thermal resistances. Thus, this cooling technology achieves high cooling performance. Similarly, Yang et al. [47], in experiments under uniform heat flux and uniform fin density, numerically and experimentally analyzed the heat transfer performance of single-phase microchannel heat sinks with five pin-fin cross-sections: triangle, square, pentagon, hexagon, and circle. Under a uniform heat flux and laminar flow of deionized water, the shapes of pin fins contribute to the balance of pressure drops and the heat transfer rate, which could achieve better cooling.

From another perspective, Sarvey et al. [48-49] developed a process to fabricate a wide range of micro-pin-fin dimensions on a silicon wafer in a single batch process. They fabricated four heterogeneous micro-pin-fin samples and found local micro-pin-fin clustering an effective method of reducing local thermal resistance with a modest pressure drop at a constant flow rate. They investigated nonuniform micro-pin-fin heat sinks for the cooling of integrated circuits with nonuniform power maps. Four heterogeneous micro-pin-fin samples were fabricated and tested in single-phase experiments with deionized water to investigate the effectiveness of local micro-pin-fin clustering for the cooling of hotspots. Cylindrical and hydrofoil micro-pin-fins samples were tested, as well as two

types of heterogeneous arrays: those with pin-fins clustered directly over the hotspot and those with the high-density cluster spanning the entire width of the channel to prevent flow bypass around the cluster. Samples were tested with a uniform nominal heat flux of 250 W/cm^2 as well as a hotspot heat flux of 500 W/cm^2. Local micro-pin-fin clustering was found to be an effective method of reducing local thermal resistance with a modest pressure drop penalty.

Lorenzini et. al [50] built a robust computational fluid dynamics/heat transfer (CFD/HT) model capable of predicting spatially resolved temperature fields arising from heterogeneous heating. Their experimental results showed that this localized or spanwise increased density cylindrical pins could maintain the maximum temperature of chips below 65°C when the temperature of the inlet coolant is maintained at 21.3°C. The CFD model provided a cost-effective thermal modeling tool for all types of power maps and pin-fin dimensions. Detailed benchmark simulations were provided to reproduce and be used for reference in numerical studies with variable pin fin densities. The described methodology represented a cost-effective thermal modeling technique for any type of heat flux distribution or power map, and IC architecture.

Several studies used various power maps to examine pin-fin structures. Abdoli et al. [51] numerically investigated the effects of distinct micro pin-fin shapes on electronic cooling with a single hotspot. These pin-fin shapes include circular, hydrofoil, modified hydrofoil, and symmetric convex shapes. The 2.45 × 2.45 mm electronic square chip with a hotspot of 0.5 × 0.5 mm at its center has a uniform heat flux of 1,000 W/cm^2 and a hotspot of 2,000 W/cm^2. They showed that compared to the cylindrical pin-fin design, the hydrofoil shape micro-pin-fin design exhibited a 30.4% reduction in pumping power and a 6.4 ºC

decrease in the maximum temperature. Shafeie et al. [52] simulated laminar forced convection water cooling in a 1 cm^2 heat sink with micro-pin-fin structures that included both oblique and staggered pin-fins structures. Their results showed that the cooling performance of the finned heat sinks was lower than that in the pin-finned microchannel heat sinks at medium and high pumping power. However, the finned heat sinks performed slightly better than the pin-finned microchannel heat sinks for small pumping power.

Brunschwiler et al. [53] tested the heat-removal capability of interlayer cooling in vertically integrated, high-performance chip stacks. They tested water as a coolant and interlayer heat-removal structures: a parallel plate, a microchannel, pin fin, and a combination of the two with pins. They used in-line and staggered configurations with round and drop-like shapes at pitches ranging from 50 to 200 μm and fluid structure heights of 100-200 μm. The performance of interlayer cooling strongly depends on this parameter.

Summarizing all these studies, liquid cooling with a pin-fin enhanced micro-gap is a promising method of providing high cooling performance. In my thesis, I would investigate if non-uniform heterogeneous pin-fins in the micro-gap could deliver enhanced localized cooling performance for heterogeneous dies, which have various configurations and power generation in the 2.5D and 3D-SICs.

1.3 Objectives and Outline

This thesis focuses on micro-gap liquid cooling with pin-fin structures for heat transfer enhancement to meet the thermal management challenges of future 2.5D and 3D-SICs. The specific topics investigated in this thesis include:

- Chapter 2: Experimental evaluation of thermal performance of heterogeneous pin-fin enhanced single-phase micro-gap liquid cooling, to accommodate spatially varying heat inputs.

- Chapter 3: Design and parametric study of a micro-gap liquid cooling manifold with dielectric coolant for aircraft application of 2.5D-SICs which include multiple heterogeneous high-power dies. Thermal and hydraulic evaluation will be performed for specially designed cooling enhancement structures in the manifold.

- Chapter 4: Systematical optimization of heterogeneous pin-fin structures in conventional cold plates to achieve non-uniform and optimized cooling capacities for multiple heterogeneous dies in 2.5D-SICs.

- Chapter 5: Development of an inter-layer liquid cooling compact thermal-electrical co-design simulation model for multi-layer 3D-SICs. From thermal perspective, the model should be able to consider spatially and temporally varying heat flux distribution, or power map, in each tier. From electrical perspective, the model should be able to simulate the leakage power and more realistic temperature distributions after deducting overestimated leakage power.

- Chapter 6: Evaluation of micro-gap thermosyphon liquid cooling for 3D-SICs. Important characteristics including power densities, effects of evaporator tilting angles, height differences between condenser and evaporator, and input chilled water temperatures for condenser are investigated, as they affect cooling performance of each layer in 3D-SICs.

CHAPTER 2. NON-UNIFORM HETEROGENEOUS PIN-FIN-ENHANCED MICRO-GAP COOLING

In this chapter, the thermal and hydraulic performance of four non-uniform heterogeneous pin-fins designs in micro-gaps are experimentally investigated for enhanced localized cooling performance evaluation. Chip temperatures, pressure drops and heat transfer coefficients of four chip designs under various uniform and non-uniform power maps have been analyzed.

2.1 Thermal Design Vehicle Configurations

In this section, the parameters of thermal design vehicles (TDVs), which include both chips with various pin-fin configurations in the micro-gap and a package that fits chips into the testing loop are introduced.

2.1.1 Chip Configurations

All chips in this chapter were fabricated by a Ph.D. candidate Thomas Sarvey at Georgia Institute of Technology with the help from clean room staffs. One of the tested chips appears in Fig. 1, which illustrates the side view of the chip in the middle of Fig. 1, the top view of the chip for the micro-gap, and the bottom view of the chip for heater sides, indicated at the bottom of Fig. 1. In the middle of the figure, the side view image shows the overall dimension of the chip, which is 2.8 cm long, 1.3 cm wide, and 0.2 cm thick. The thickness includes both a silicon layer with a micro-gap and a glass layer covered on the top of the silicon gap as a gap roof. With the transparent glass, the top view of the chip, listed in the top of Fig. 1, shows the etched silicon gap, indicated by a blue dashed line, and tested pin-fin areas of 1 cm x 1cm in the gap, indicated by a yellow dashed square. In

the etched gap area, two holes with a diameter of 1.2 mm are etched through and serve as an inlet and an outlet for coolant. Pins with a diameter of 0.5 mm serve as a gap-supporting structures are located around the inlet and the outlet. These supporting structures are two areas, one located upstream of the tested pin-fin area and the other downstream. A mini-pressure 0.8 μm port, located both upstream and downstream of the tested pin-fin area, measures the pressure drop across the tested pin-fin area. Opposite this tested area, five platinum resistance heaters are fabricated on the bottom side of the silicon layer, shown in the bottom of Fig. 3. The total area of heaters, 1 cm x 1cm, includes four background heaters and a 0.25 mm^2 square hotspot in the center. The resistances of these five platinum heaters are calibrated and measured by a multimeter in an oven at 20, 40, 60, 80, 100, and 110 ºC. Fig. 4 shows an almost linear correlation of temperature and resistance of one heater in a temperature range from 20 to 110 º C. Temperatures of all five heaters can be converted from their resistance measurements during the heating process in the experiments. Thus, these five heaters serve both heating elements as well as temperature sensors by measuring their resistance.

Four background heaters and a hotspot heat the tested area with four designs of non-uniform heterogeneous fins. Table 1 illustrates the four designs of the test areas, two of which have cylindrical fins and the other two have hydrofoil fins. Both cylindrical and hydrofoil fins have one design with increased fin density around the hotspot only and the other with increased fin density spanning along the entire width of the channel. In total, four chips were tested with the four designs of the test areas. The coolant, deionized water, flows through the test areas, indicated by a black arrow in Table 1, which also shows images of partial enlargements of the hotspot areas from a scanning electron microscope. Table 2 lists the configurations of the fin arrays, such as fin heights, diameters and pitches, in the tested areas for all four designs.

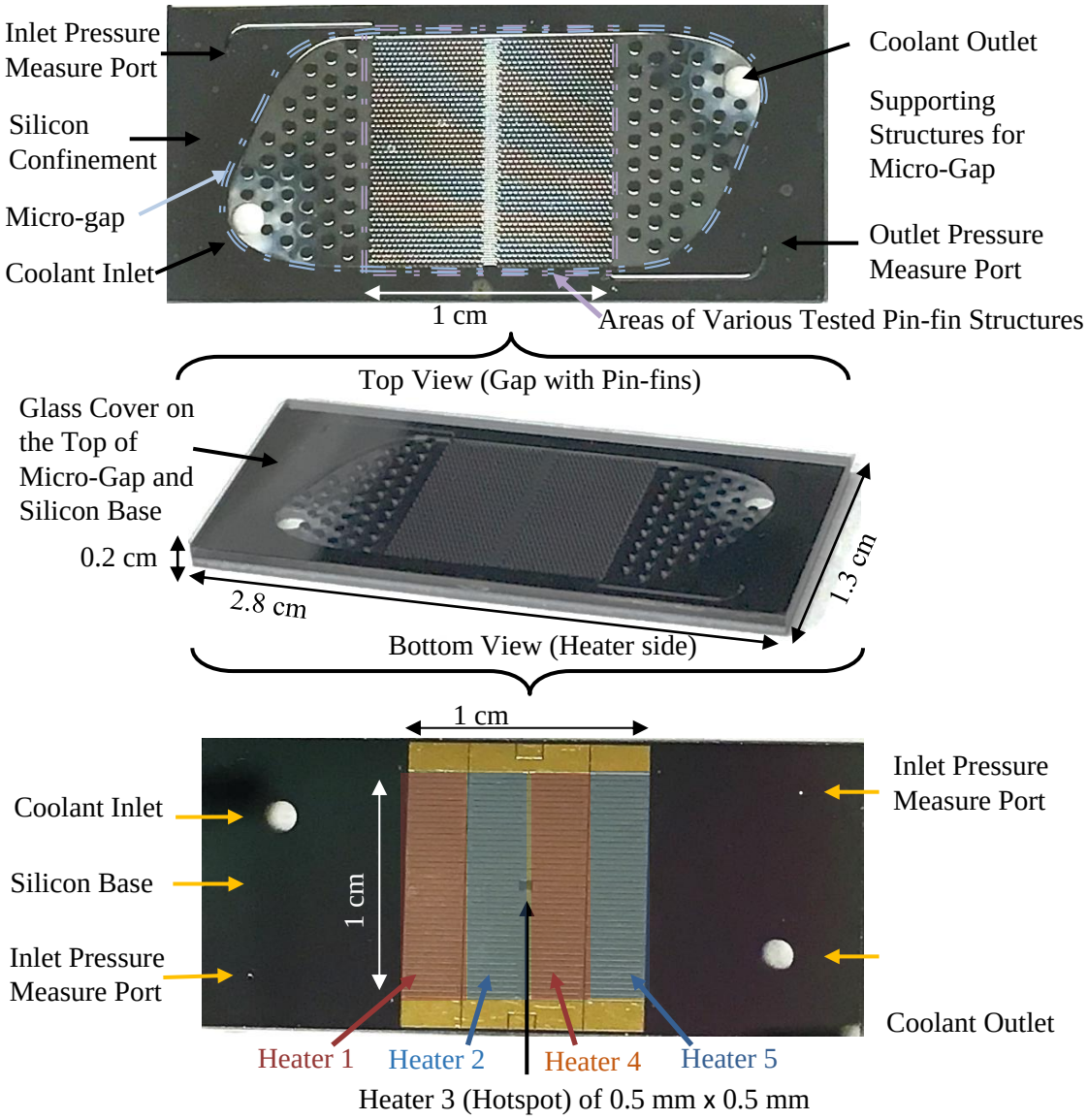
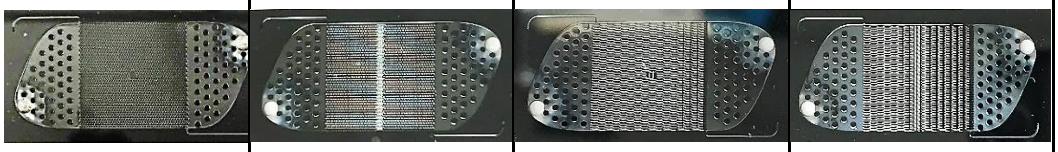
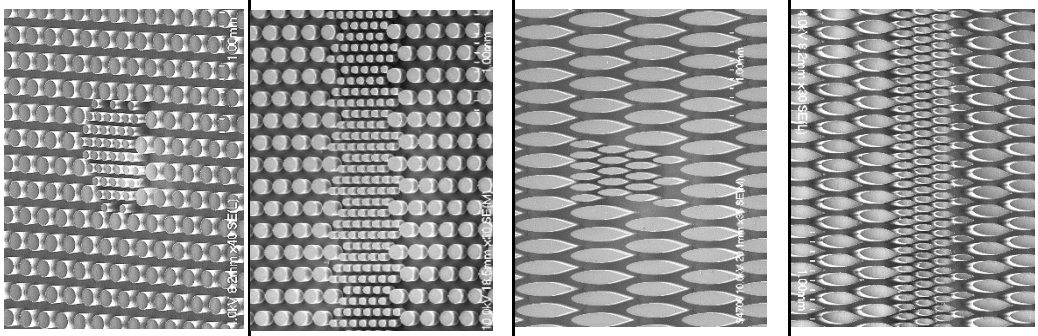


Figure 3: A tested chip illustration that includes the top micro-gap side with pin-fins and a bottom heater side.

Table 1: Channel-side designs of various chips.

	Chips with Cylindrical Pins		Chips of Hydrofoil Fins	
Four Types of Chips	Hotspot Cluster	Spanwise Direction	Hotspot Cluster	Spanwise Direction
	Flow Directions of All Chips: ➡			
				
Partial Enlargements of Hotspot				

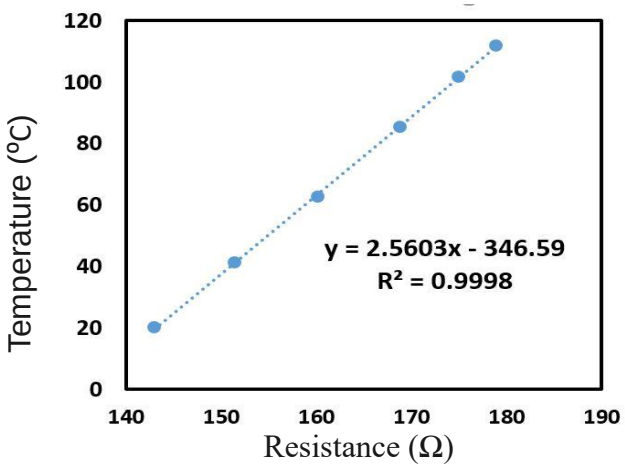


Figure 4: Calibration of platinum resistance thermometers.

Table 2: Parameters of fin arrays with various chip designs.

Unite: μm	Chips with cylindrical fins		Chips of hydrofoil pins	
Heights of fins (H)	200			
Unite: μm	Normal density area	Increased density area	Normal density area	Increased density area
Diameters of fins (D)	150	75	D_{tr}=150; D_{lg}=714	D_{tr}=75; D_{lg}=357
Pitches (S_{tr})	225	112.5	225	112.5
Pitches (S_{lg})	225	112.5	N/A	N/A

2.1.2 Package Configurations

To enable chip-performance testing, Xuefei Han and I designed a package that adapts to chips and enables them to be tested as a thermal design vehicle (TDV) in the liquid testing loop. Fig. 5 illustrates a wire-bonded chip on a plastic circuit board (PCB), a package, and the assembling process of both. The chips are tested with five heaters, wire-bonded to the PCBs, one case depicted in Fig. 5 (a). Thus, all heater terminals are connected to the PCB terminals, wired to five power supplies and a data collector that generates power and measures resistances. All resistances of the heaters are converted into chip temperatures via platinum resistance calibration curves. The chip attached to the PCB, indicated in the figure, has been placed on top of the package made of polyether ether ketone. The package has one flow channel with a larger diameter for the liquid loop as well as two smaller pressure-monitor channels connected to the pressure sensors. Fig. 5 (a) indicates the inlet and outlet ports and two smaller pressure-monitor ports by a dash rectangular. The four ports are connected to the chip. At the locations of the connections,

O-rings were placed, which prevent leaking. Two k-type thermocouples were inserted into the flow channel of the package, one before and one after the chip to measure coolant temperatures before and after the tested chip. Fig. 5 (b) illustrates an assembled TDV with the wire-bounded chip and package. These parts are assembled by four bolts and nuts for TDV integrity and air tightness.

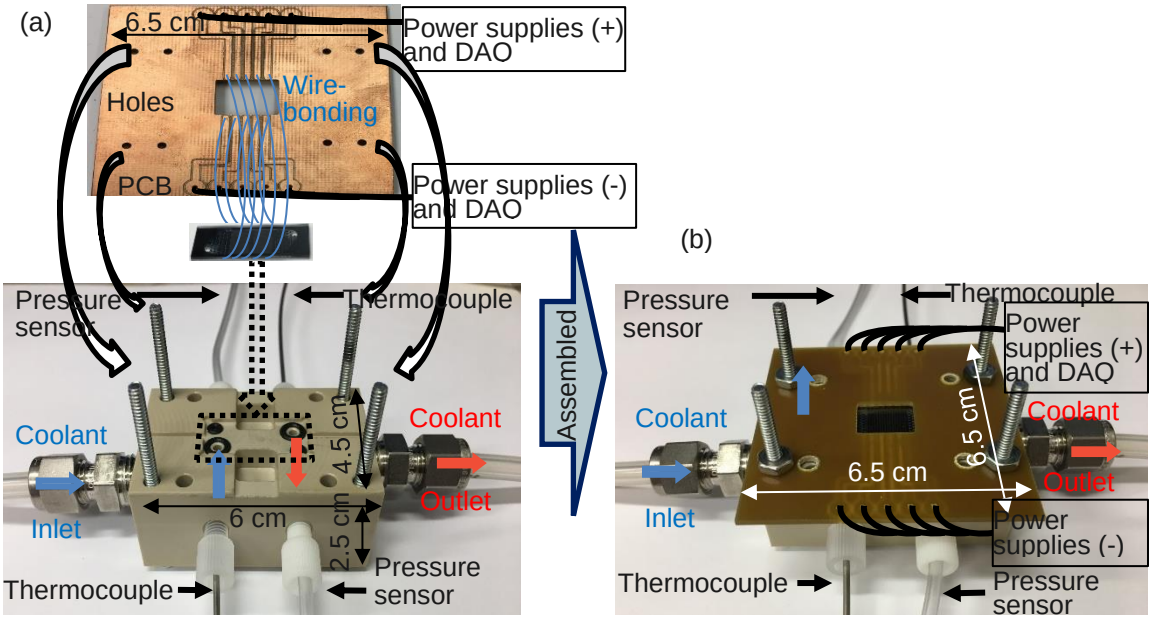


Figure 5: TDV assembled by a chip and a package: (a) a package, a chip, and a plastic circuit board; (b) an assembled TDV.

2.2 Experimental Setup and Power Maps of Heaters

Using de-ionized (DI) water, the single-phase liquid-cooling performance of the four chip designs in an opened-loop experimental setup were tested, as depicted in Fig. 6. DI water was pumped (digital gear pump) as coolant through a flow meter, the TDV with five power supplies, and the data collectors mentioned in Fig. 5, and eventually into a reservoir. To monitor the coolant temperatures and pressure drop caused by the fin arrays in the chip of the TDV, pressure gauges (COMARK, C9557, 0-1379 kPa) and K-type thermocouples (Diameter=0.48 mm) were connected to the inlet and the outlet of the TDV.

Various power maps provided by power supplies are listed in Table 3, which also lists the ratios of the hotspot power to the power of a background heater.

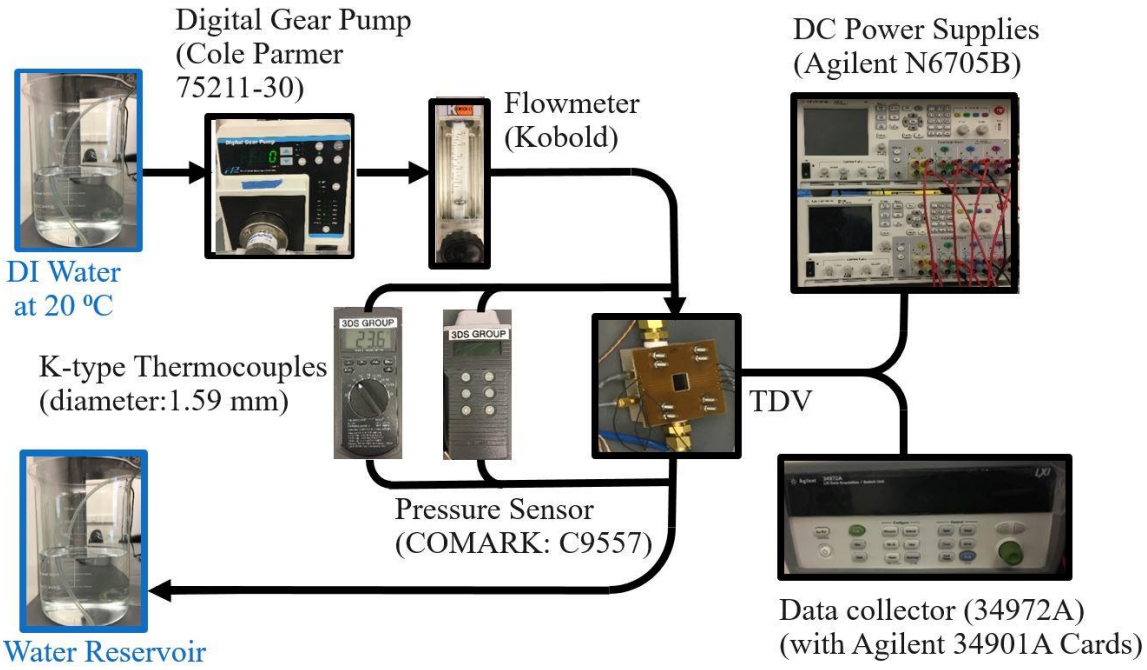


Figure 6: The experimental setup for the single-phase liquid cooling of the heterogeneous pin-fin-enhanced micro-gap with non-uniform fin arrays.

Uncertainties are estimated by combining the precision and bias components. The uncertainty of the pressure sensor (COMARK: C9557) was acquired using Omega, DPI 610. Uncertainties of the flow rates were acquired by repeatedly measuring the flow volume under constant time. The uncertainties of K-type thermocouples were measured with a mercury thermometer in a mixture of ice and water, and hot water at 20 ºC, 40 ºC, 60 ºC, and 100 ºC.

Table 3: Various tested power maps.

Power of a background heater (W/cm^2)	Hotspot power (W/cm^2)	Power ratios of the hotspot and a background heater
125	125	1
250	250	1
125	250	2
250	500	2
325	650	2
250	750	3
125	500	4
125	625	5

Table 4: Measurements of uncertainties.

Parameters	Uncertainty value
Pressure	$\pm$0.1 kPa
Flow rate	$\pm$ 0.8 ml/min
Coolant temperature	$\pm$0.4 ℃
Heat flux	$\pm$0.1 W/cm^2

2.3 Experimental Results

Thermal and hydraulic experimental results of these four non-uniform heterogeneous pin-fins designs in micro-gaps are presented in this section. These thermal and hydraulic results include chip temperatures, heat transfer coefficients and pressure drops of four chip designs under various uniform and non-uniform power maps.

2.3.1 Cylindrical Pin Fins

To ensure identical conditions in the experiments, a steady-state compact model [30-31] were used for a micro-gap with uniform cylindrical pins as a baseline. This compact model rapidly simulates micro-gap liquid cooling with uniform cylindrical pin-fins. It entails power maps, and various flow velocities and directions. This compact model has been verified by CFD/HT simulations, and applied in design space exploration in thermo-electric feasibility regions, which can optimize energy efficiency and performance inside these regions.

The same pin-fin configurations as those in the experiments indicated in Table 2 were set to use the results of this simulation model as a baseline for comparison with our experimental results. The only difference between the pin-fin configurations in simulation case and those of the experiments is the pin-fin arrangement: a uniform fin-pin density in the simulation without enhanced-density pin-fins. For two experimental chips with different pin arrangements. One chip has an increased pin density only around the hotspot area, listed in the first column of Table 1, and the other has increased pin-fin density along the entire spanwise width of the channel, listed in the second column of Table 1. Fig. 7 (a) presents both experimental results of these two chips and the simulation result with uniform pin configuration under a uniform power map 250 W/cm^2. Results from one experimental chip with an increased pin density only around the hotspot area, indicated by black dots,

and results from the other with increased pin-fin density along the entire spanwise width of the channel, indicated by green dots. In addition to these two sets of experimental results, the set of simulation results, as a baseline for comparison with the experimental results, is depicted by a black dashed line, which shows that the temperatures of the chip increase linearly from upstream to downstream under the uniform pin arrangement. In the two experimental sets, however, the temperatures of the hotspot drop dramatically because of the localized increased pin-fin density. The hotspot temperature in the increased cylindrical spanwise pin density case is the lowest, indicating better cooling performance of this pin-fin structure under the same flow rate of Q=8.56 L/hr.

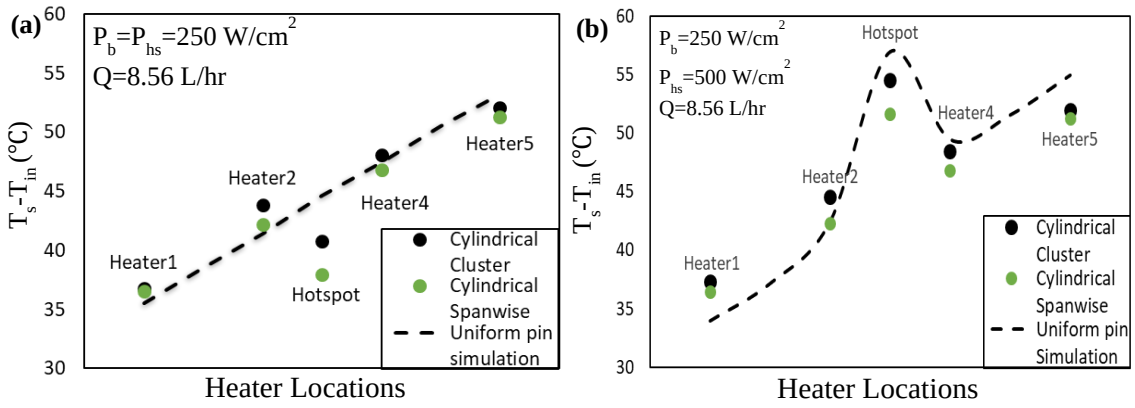


Figure 7: Temperature differences of chips and coolant inlets with two cylindrical pin-fin arrangements from experiments and one uniform cylindrical pin arrangement from simulation: (a) P_b=P_{hs}=250 W/cm^2, Q=8.56 L/hr; (b) P=250 W/cm^2, P_{hs}=500 W/cm^2, and Q=8.56 L/hr.

2.3.2 Comparison of the Results of All Four Chip Designs of the Experiments

In addition to the uniform power map, a power map with a hotspot was applied: All of the background heaters at 250 W/cm^2, and the hotspot heater at 500 W/cm^2. Temperature difference between chips and inlets from the simulations and experiments are shown in Fig. 7 (b) under the same flow rate for both the simulation and experiments. Similar to Fig. 7 (a), the experimental sets exhibit increased pin density only around the

hotspot area, indicated by dark dots, and the other shows increased pin-fin density along the entire spanwise width of the channel, indicated by green dots. Simulations were performed and a set of simulation results was displayed as the baseline by a black dashed line. This figure indicates that among all three sets of results, the temperatures of all the background heaters increase from upstream to downstream; however, the temperatures of hotspots located in the center of the chips are the highest, owing to the doubled power in that area. It is worth noting that both experimental temperatures of hotspots with enhanced pin densities are lower than the hotspot temperature simulated without increased pin density, showing better cooling performance of the two experimental tested pin designs. Particularly, the design with cylindrical spanwise increased pins has a lower temperature under the hotspot power map, suggesting that this chip design has better cooling performance than that the design with the only increased pin density in the hotspot area and the design of the uniform cylindrical pins under a constant flow rate of Q=8.56 L/hr.

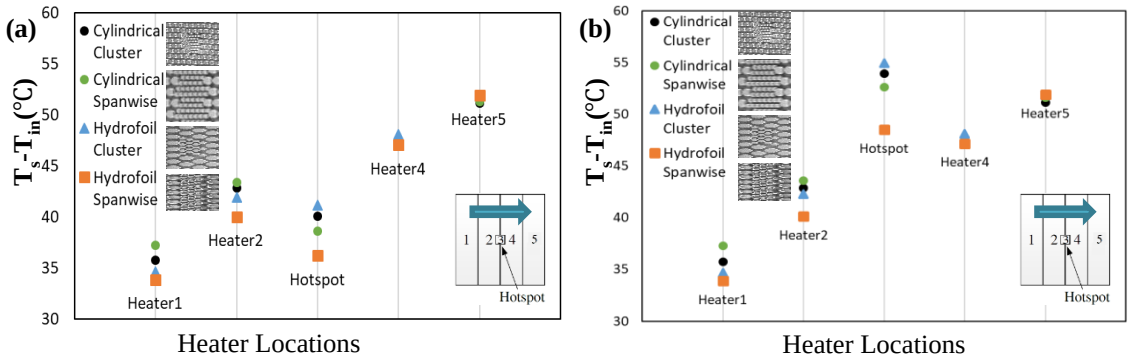


Figure 8: Temperature differences of chips and coolant inlets with various pin-fin arrangements from experiments at Q=8.56 L/hr: (a) P_b= P_{hs}=250 W/cm^2; (b) P_b=250 W/cm^2 and P_{hs}=500 W/cm^2.

Fig. 8 entails temperature differences of all four heterogeneous chips and their coolant inlets. Results of chip with an increased cylindrical pin density only around the hotspot area are indicated by black dots, and results from the chip with increased cylindrical pin density along the entire spanwise width of the channel are indicated by green dots. In

addition to these results of cylindrical pin designs, results of chip with an increased hydrofoil fin density only around the hotspot area are indicated by blue triangles, and results from the chip with increased hydrofoil fin density along the entire spanwise width of the channel are indicated by orange squares. Fig. 8 (a) presents temperatures from designs under uniform power map of $P_b = P_{hs} = 250$ W/cm^2. Temperatures of background heaters linearly increase from upstream to downstream for all chips. Before hotspots in the center, two upstream background heaters of two cases with cylindrical pins have higher temperatures than the cases with hydrofoil fins, which indicates better cooling performance of the hydrofoil fin design. For temperatures of hotspots, all of them are lower than their neighbor background heaters, because of the uniform power density with higher pin-fin densities. The temperatures of the two designs with cylindrical fins, falling between those of the designs with hydrofoil fins, are similar.

The design with hydrofoil spanwise case has the best cooling performance because of its lowest temperature. However, another hydrofoil fin design with increased density only around the hotspot area, called hydrofoil cluster, has the highest temperature. A higher portion of the flow goes around the cluster could contribute to the worst cooling hotspot cooling performance of this hydrofoil cluster design. Fig. 8 (b) presents temperatures under identical design configurations in Fig. 8 (a), but with power map of P_b=250 W/cm^2 and P_{hs}=500 W/cm^2. Like the results of Fig. 8 (a), temperatures of background heaters linearly increase from upstream to downstream for all chips. Before hotspots in the center, two upstream background heaters of two cases with cylindrical pins have higher temperatures than the cases with hydrofoil fins, which indicates better cooling performance of the hydrofoil fin design. For temperatures of hotspots, all of them are higher than their neighbor background heaters, owing to the doubled power in that area. The temperatures of the two designs with cylindrical fins, falling between those of the designs with hydrofoil fins, are similar. Hotspot temperatures of all the designs, except the hydrofoil spanwise

one, are higher than the temperatures of their background heaters, which indicate these enhanced cooling designs for hotspots are not efficient enough to compensate the doubled power. Although the design with hydrofoil spanwise case does not compensate the doubled power either, this design has the best cooling performance among all designs with the lowest hotspot temperature that is lower than the temperature of downstream background heater 5.

2.3.3 Temperatures under Power Ratios of a Hotspot to Background Heaters

In additional to the two power maps indicated in Fig. 8, all the chip designs under various power maps were tested to investigate the hotspot cooling performance of these designs under various conditions. Fig. 9 shows the hotspot temperatures with various power ratios of the hotspot to a background heater under a flow rate of 11.44 L/hr. The horizontal axis shows power density ratios from 1 to 5, and the vertical axis shows temperature differences between the hotspots and the coolant at the inlet. Power densities of background heaters are 125 W/cm^2. All four pin-fin designs were experimentally tested, including cylindrical pins and hydrofoil fins with increased fin density around the hotspot only and cylindrical pins and hydrofoil fins with increased fin density spanning along the entire width of the channel.

For all ratios, the hotspot temperatures of a design with increased hydrofoil fin density spanning along the entire width of the channel are the lowest, and those of the design with a cluster-increased hydrofoil fin density only around hotspot areas are the highest. In addition, the temperatures of the two designs with cylindrical fins, falling between those of the designs with hydrofoil fins, are similar. With increasing ratios along the horizontal axis, all hotspot temperatures increase. In addition, the chip design with the increased hydrofoil fin density spanning the entire width of the channel exhibits increasingly lower temperatures relative to those of the other designs. Thus, because of its

increasingly lower relative temperature with increasing power ratios of the hotspot and the background heater, this chip design is a better choice for cooling.

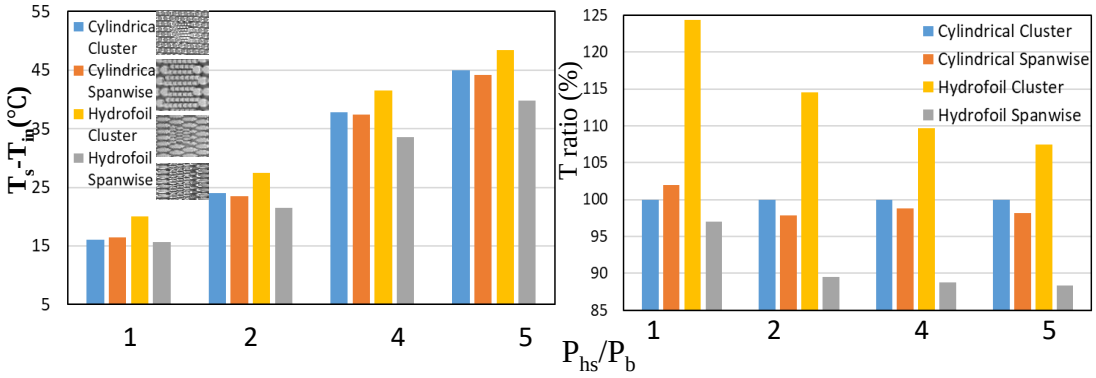


Figure 9: Cooling performance for hotspots of various designs with power density ratios of the hotspot to a background heater from 1 to 5 with P_b =125 W/cm^2, under a flow rate of 11.44 L/hr: (a) Temperature differences of chips and coolant inlets; (b) temperature difference ratios of various pin-fin arrangements to cylindrical cluster case.

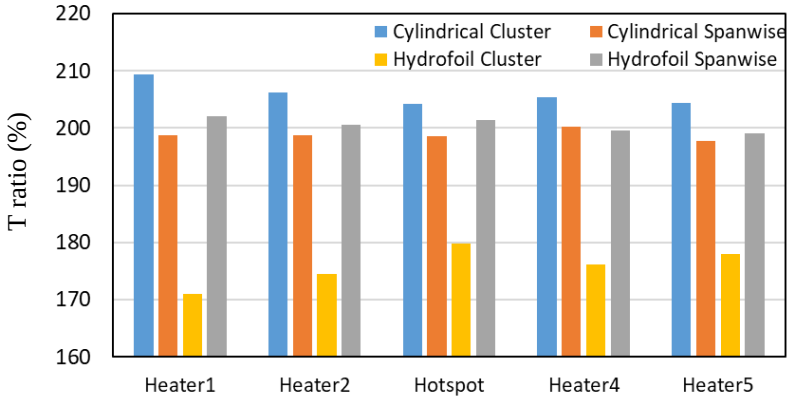


Figure 10: Effects of doubled power to chips at Q=8.56 L/hr: Ratios represent the chip temperatures with P_{hs}=500 W/cm^2 and P_b=250 W/cm^2, to chip temperatures with P_{hs}=250 W/cm^2 and P_b=125 W/cm^2.

Compared to various power density ratio of the hotspot to a background heater, Fig. 10 presents the temperate ratios of all chip designs under two power maps which have the same power density ratio as two, but with different total power. One power map has the

background power density as 125 W/cm^2 and hotspot as 250 W/cm^2, and the other has doubled power densities with the background power density as 250 W/cm^2 and hotspot as 500 W/cm^2. With the doubled power densities, temperature ratios of all background heaters and the hotspot have been shown in Fig. 10. In the hydrofoil cluster design, indicated by yellow bars, the temperatures of background heater increased to 170-178% of the lower power map case, and the hotspot temperature increased to 180% of the lower power map case. Although the hotspot temperature increasing rate is higher than those of background heaters, all heaters' temperature increasing rates are lower than those of other three chip designs, which have about 200% increasing rate for all their heaters. Compared to other designs, hydrofoil cluster design has a better cooling capacity with increasing power, which is even competitive to other designs.

2.3.4 Heat Transfer Coefficients

In addition to the temperature analyses of various chip designs, localized heat transfer coefficient analyses have been performed in this section, considering cooling effect of various heat transfer areas in these designs. Localized heat transfer coefficients of heaters have been calculated by the equation listed below:

	$$\boldsymbol{h_l = \frac{P_l}{A_c(T_s - T_{in})}}$$	(1)

where $\boldsymbol{P_l}$ is the set of localized power provided for each heater, including the hotspot; $\boldsymbol{A_c}$ is the set of heat transfer areas between coolant and silicon surfaces, including the channel bases with heaters and pin-fin surfaces; $\boldsymbol{T_s}$ is the set of heater surface temperatures, and $\boldsymbol{T_{in}}$ is the set of coolant inlet temperatures of each design case. $\boldsymbol{A_c}$ of all hot spot areas and background heater areas in all four designs have been presented in Table 5.

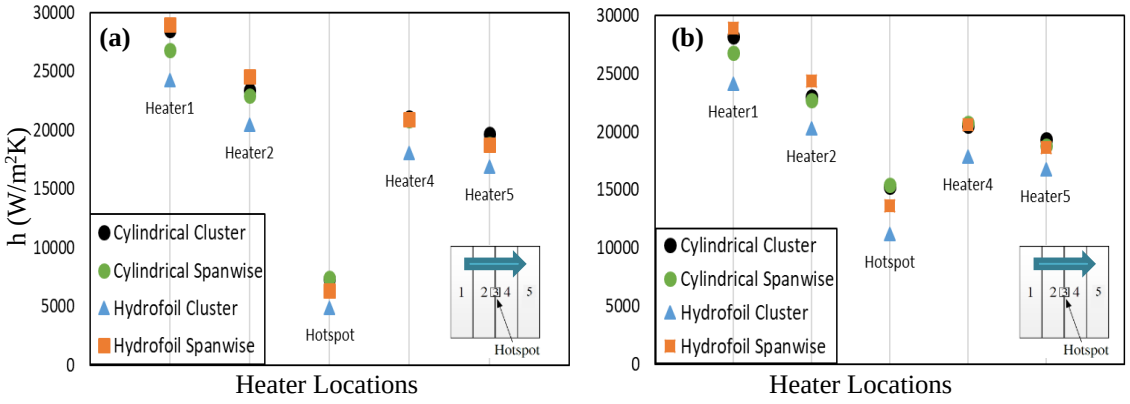


Figure 11: Local heat transfer coefficients of various pin-fin arrangements under a constant flow rate of Q=8.56 L/hr. Power densities: (a) P_b=P_{hs}=125 W/cm^2; (b) P_b=125 W/cm^2 and P_{hs}=625 W/cm^2.

Table 5: Contacted areas of heaters in four designs.

A_c (m^2)	Heater 1	Heater 1	Hotspot	Heater 1	Heater 1
Cylindrical Cluster	6.2 x 10^{-5}	6.2 x 10^{-5}	1.1 x 10^{-6}	6.2 x 10^{-5}	6.2 x 10^{-5}
Cylindrical Spanwise	6.2 x 10^{-5}	7.1 x 10^{-5}	1.1 x 10^{-6}	7.1 x 10^{-5}	6.2 x 10^{-5}
Hydrofoil Cluster	6.4 x 10^{-5}	6.4 x 10^{-5}	1.4 x 10^{-6}	6.4 x 10^{-5}	6.4 x 10^{-5}
Hydrofoil Spanwise	6.4 x 10^{-5}	7.7 x 10^{-5}	1.4 x 10^{-6}	7.0 x 10^{-5}	6.4 x 10^{-5}

Fig. 11 presents heat transfer coefficients of heaters in all four heterogeneous chips. Compared to chip temperatures presented before, these heat transfer coefficients consider shape-effects of pin-fins, because of considering the effective cooling area. Results of chip with an increased cylindrical pin density only around the hotspot area are indicated by black dots, and results from the chip with increased cylindrical pin density along the entire

spanwise width of the channel are indicated by green dots. In addition to these results of cylindrical pin designs, results of chip with an increased hydrofoil fin density only around the hotspot area are indicated by blue triangles, and results from the chip with increased hydrofoil fin density along the entire spanwise width of the channel are indicated by orange squares.

Fig. 11 (a) presents heat transfer coefficients of heaters under uniform power map of $P_b = P_{hs} = 125$ W/cm^2. Heat transfer coefficients of background heaters decrease from upstream to downstream for all chip designs. In contrast to the lowest heat transfer coefficients of hydrofoil cluster design, all other three sets of heat transfer coefficients of their designs are similar after their hotspots. For heat transfer coefficients of hotspots, all of them are lower than their neighbor background heaters, because of the increased contact areas under uniform power density. In this hotspot location, two cylindrical pin designs have similar contact area, which are smaller than the same contact areas of two hydrofoil fin designs. The heat transfer coefficients of the two designs with cylindrical fins are similar and highest, because of the smaller contact areas compared to cylindrical designs. However, two hydrofoil fin designs with same contact area do not have a similar heat transfer coefficient. The design with hydrofoil cluster case has the lowest heat transfer coefficient because of its higher temperature. The heat transfer coefficient of another hydrofoil fin design with increased density along the entire spanwise width of the channel, called hydrofoil spanwise, has fallen between these of other designs.

Fig. 11 (b) presents heat transfer coefficients under identical design configurations in Fig. 11 (a), but with power map of P_b=125 W/cm^2 and P_{hs}=625 W/cm^2. Heat transfer coefficients of background heaters linearly decrease from upstream to downstream for all chips, which are similar to the results of Fig. 11 (a) because of the same background power densities. For the hotspot location, similar to Fig. 11 (a), the heat transfer coefficients of the two designs with cylindrical fins are similar and highest as well. The heat transfer

coefficient of the hydrofoil cluster case has the lowest heat transfer coefficient, and the heat transfer coefficient of another hydrofoil spanwise design has fallen between these of other designs. However, compared to uniform power map condition, the heat transfer coefficients have raised to the range of 10,000 to 15,000 W/m^{2}K, instead of 4,000 to 7,000 W/m^{2}K because of five times higher local power densities.

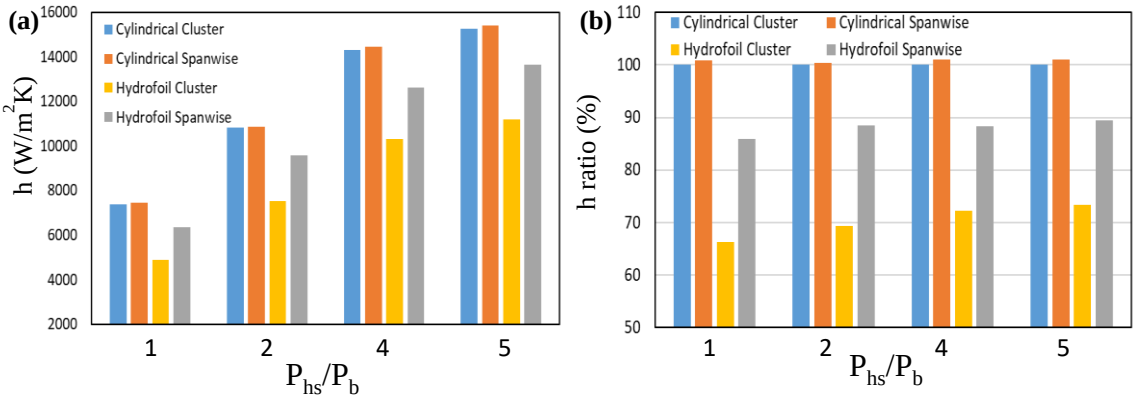


Figure 12: Heat transfer coefficients of hotspots with various pin-fin arrangements under a constant flow rate of Q=8.56 L/hr, and power density ratios of the hotspot to a background heater from 1 to 5 with P_b =125 W/cm^2; (b) heat transfer coefficient ratios of various pin-fin arrangements to cylindrical cluster case, under the same condition in (a).

In additional to the heat transfer coefficients of all heaters with two power maps indicated in Fig. 11, all the chip designs under various power maps were tested to investigate the hotspot heat transfer coefficient of these designs under various conditions. Fig. 12 shows the heat transfer coefficients with various power ratios of the hotspot to a background heater under a flow rate of 8.56 L/hr. The horizontal axis shows power density ratios from 1 to 5, and the vertical axis shows heat transfer coefficients of hotspots. Power densities of background heaters are 125 W/cm^2. With increasing ratios along the horizontal axis in Fig. 12 (a), all heat transfer coefficients of hotspots in all chip designs increase. Among these chip designs, the design of cluster-increased hydrofoil fin density only around hotspot areas has the lowest heat transfer coefficients among all power density ratios. These

lowest heat transfer coefficients increasing from 4,895 W/cm^{2}K to 11,185 W/cm^{2}K with the increasing of hotspot power ratio. On the contrary, the cylindrical spanwise chip design has the highest heat transfer coefficients from 7,451 W/cm^{2}K to 15,418 W/cm^{2}K with the increasing power ratio of hotspot to the background. Heat transfer coefficients are in the range of 4,895 to 7,451 W/cm^{2}K with all designs under the power ratio of 1.

When the power ratio increases to 5, the heat transfer coefficients of hotspots are in the range of 11,185 to 15,418 W/cm^{2}K, which is twice of the heat transfer coefficients with power ratio of 1. For heat transfer coefficient comparison of chip designs under the same power ratio, Fig 8 (b) sets heat transfer coefficients of cylindrical cluster chip design as the baseline for other designs. The relative heat transfer coefficient ratio of cylindrical spanwise design keeps constant at 101% for all the power ratio. However, the relative heat transfer coefficient ratio of hydrofoil cluster design increase from 66% to 73% with the increasing of power ratio. Similarly, the relative heat transfer coefficient ratio of hydrofoil spanwise case increase from 86% to 90%. Thus, the heat transfer coefficients increase with the increasing of hotspot power ratio, but the relative heat transfer coefficient ratio of cylindrical spanwise design keep constant, while hydrofoil designs increase.

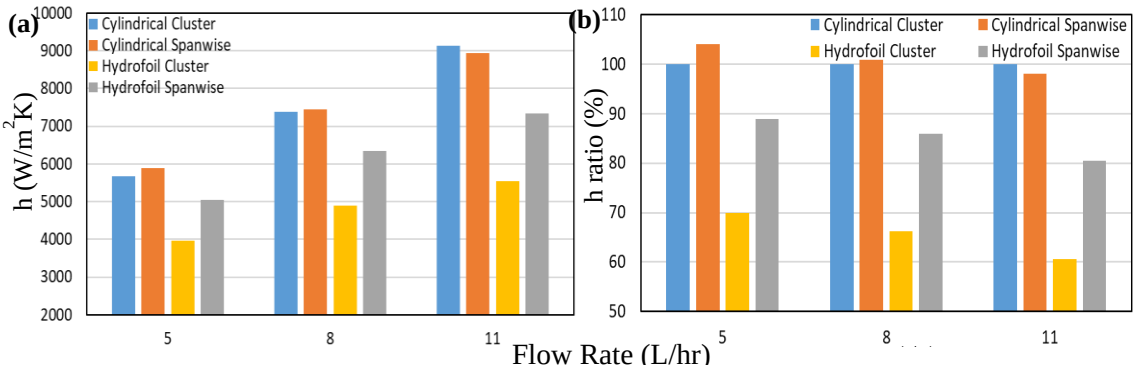


Figure 13: Heat transfer coefficients of hotspots with various pin-fin arrangements with P_b=P_{hs}=125 W/cm^2 under flow rates from 5 to 11 L/hr; (b) heat transfer coefficient ratios of various pin-fin arrangements to cylindrical cluster case, under the same condition in (a).

Hotspot heat transfer coefficients of all chip design were also investigated with the uniform power density under various flow rates, as indicated in Fig. 13. With increasing flow rate along the horizontal axis in Fig. 13 (a), all heat transfer coefficients of hotspots in all chip designs increase. Among the two cylindrical pin designs, which always have higher heat transfer coefficients, the design of spanwise-increased cylindrical pin density has the highest heat transfer coefficients at lower flow rates of 5 and 8 L/hr, the other design of cluster cylindrical pin density only around hotspot areas has the highest heat transfer coefficients of 9,127 W/cm^{2}K at higher flow rate of 11 L/hr. Among two hydrofoil fin designs, which have lower heat transfer coefficients, the hydrofoil cluster design has the lowest heat transfer coefficient ranging from 3,963 to 5,533 W/cm^{2}K with the increasing of flow rate. From flow rate of 5 to 11 L/hr, heat transfer coefficients of cylindrical cluster and cylindrical spanwise design increase 3,460 and 3,055 W/cm^{2}K, however, hydrofoil cluster and hydrofoil spanwise design only increase 1,570 and 2,308 W/cm^{2}K. For heat transfer coefficient comparison of chip designs under the same flow rate, Fig 13 (b) sets heat transfer coefficients of cylindrical cluster chip design as the baseline for other designs. The relative heat transfer coefficient ratios of cylindrical spanwise design decrease from 104% to 98% with the increasing of flow rate. Similarly, the relative heat transfer coefficient ratio of hydrofoil spanwise design and hydrofoil spanwise design decrease from 89% to 80% and 70% to 61%, respectively. Thus, with a uniform power density P_b=P_{hs}=125 W/cm^2, the cylindrical cluster design has the maximum heat transfer coefficients at higher flow rate, the cylindrical spanwise design would be maximum at lower flow rates. Relative heat transfer coefficients of both hydrofoil designs decrease with the increasing of flow rate.

After investigating the hotspot heat transfer coefficients of all chip design with uniform power density under various flow rates, the hotspot heat transfer coefficients of all chip design with nonuniform power density, P_b=125 W/cm^2 and P_{hs}=625 W/cm^2, were

studied as indicated in Fig. 14. With increasing flow rate along the horizontal axis in Fig. 14 (a), all heat transfer coefficients of hotspots in all chip designs increase. Among all the designs with various flow rates, the one of spanwise-increased cylindrical pin density always has the highest heat transfer coefficients from 13,821 to 16,604 W/cm^{2}K with the increasing of flow rate from 5 to 11 L/hr. The hydrofoil cluster design always has the lowest heat transfer coefficient ranging from 10,154 to 11,956 W/cm^{2}K with the increasing of flow rate. In contrast with the different increasing amount of heat transfer coefficient with increasing of flow rate under uniform power map, indicated in Fig. 13, heat transfer coefficients of all these designs increase the same mount about 2,000 W/cm^{2}K with the flow rate increasing from 5 to 11 L/hr.

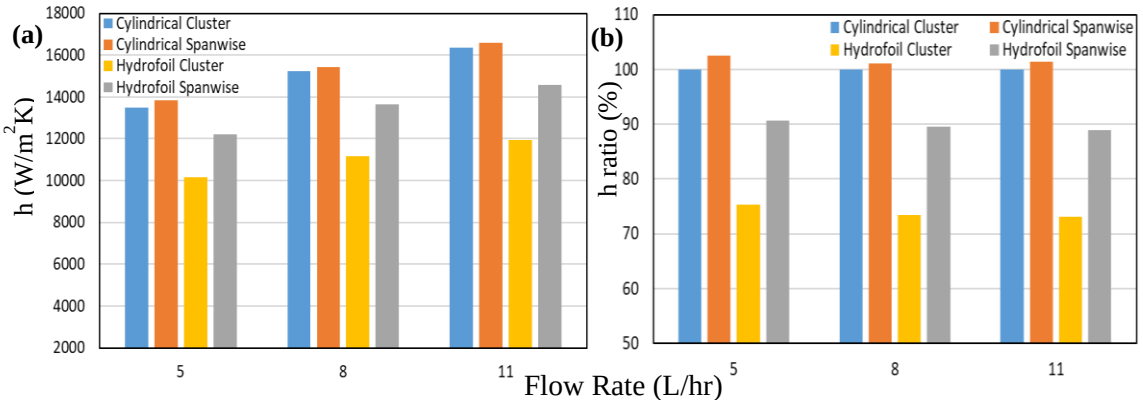


Figure 14: (a) Heat transfer coefficients of hotspots with various pin-fin arrangements with P_b=125 W/cm^2 and P_{hs}=625 W/cm^2 under flow rates from 5 to 11 L/hr; (b) heat transfer coefficient ratios of various pin-fin arrangements to cylindrical cluster case, under the same condition in (a).

For heat transfer coefficient comparison of chip designs under the same flow rate, Fig 13 (b) sets heat transfer coefficients of cylindrical cluster chip design as the baseline for other designs. The relative heat transfer coefficient ratios of cylindrical spanwise design keep constant around 102% under various flow rates. Similarly, the relative heat transfer coefficient ratio of hydrofoil spanwise design and hydrofoil spanwise design just decrease slightly from 91% to 89% and 75% to 73%, respectively. Thus, with hotspot power map,

P_b =125 W/cm^2 and P_{hs} =625 W/cm^2, the cylindrical cluster design has the maximum heat transfer coefficients. Higher flow rates contribute to higher heat transfer coefficients, but do not affect the relative heat transfer coefficients among these designs under the same flow rate.

2.3.5 Pressure Drops

Pressure drops of these four chip designs at various flow rates were investigated, as indicated in Fig. 15 (a). In addition to the absolute values of pressure drop, Fig. 15 (b) compares these pressure drops at each flow rate and present these relative pressure drop ratios of these four designs. The pressure drops of cylindrical cluster design that has pins with increased pin density around the hotspot only, are used as baselines for comparisons. In Fig. 15 (a), pressure drops of all chip designs increase linearly with higher flow rate. At each flow rate, two designs with increased pin-fin density along all the spanwise have higher pressure drops due to larger intensive pin-fin areas. Pressure drop comparisons of all these designs are presented in (b) for various flow rates. At any constant flow rate, the hydrofoil spanwise increased density design, indicated by grey bars, has the highest pressure drop, which is as much as 143% of those with the baseline design, indicated by a blue bar at a flow rate of Q=5.2 L/hr. These blue bars represent the design of the cylindrical cluster have the lowest pressure drops in most of the lower flow rate cases.

As the flow rates increase, the design of the hydrofoil spanwise increased density case, compared to the baseline design with enhanced cylindrical pin density around the hotspot, still undergoes the highest pressure drop, but its relative pressure drops decrease from 143% to 122%, which indicates a better usage condition for the hydrofoil spanwise design. For the orange bars, the design of cylindrical pins with increased pin density along all the spanwise, they have the second highest pressure drops among four designs at any flow rate. The yellow bars that are the second lowest in most of the lower flow rate cases,

represent the pressure drops of the design with enhanced hydrofoil fin density around the hotspot only. In addition, as the flow rate increasing, compared to the relative pressure drops of the baseline, those of the design with enhanced hydrofoil fin density around the hotspot decrease from 115% to 98%, which are even lower than the pressure drops of the baseline design with enhanced cylindrical pin density around the hotspot.

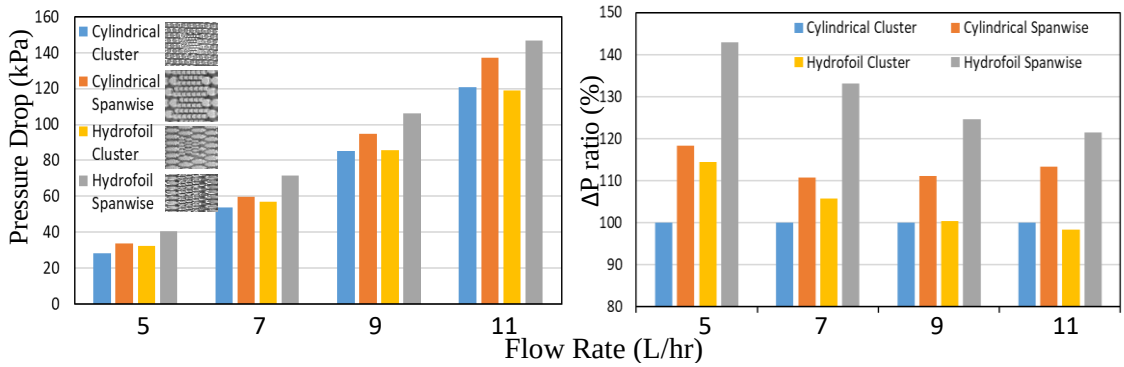


Figure 15: (a) Pressure drops of all chip designs under various flow rates P_b=250 W/cm^2 and P_{hs}=500 W/cm^2; (b) Power drop ratios of various pin-fin arrangements to cylindrical cluster case under the same situation in (a).

2.4 Summary

In Chapter 2, hot spot thermal management of micro-gap liquid cooling using non-uniformed heterogeneous pin-fin has been performed experimentally.

These four tested chip designs with non-uniform heterogeneous pin-fin are two chip designs with cylindrical fins and the other two with hydrofoil fins. Both cylindrical and hydrofoil fins have one design with increased fin density around the hotspot only and the other with increased fin density spanning along the entire width of the channel. In total, four chips were tested with the four designs of the test areas. Four background heaters provide varying but uniform power, while another small heater serves as a hotspot with varying power.

The experiments and simulation presented in this chapter demonstrate that the non-uniform pin-fin density in the micro-gap could contribute to better cooling performance for hot spots. For cylindrical pin-fin structure, increased fin density spanning along the channel width yields a lower hotspot temperature. As the power ratio increases, the hydrofoil spanwise design has an increasingly low relative temperature. It exhibited the best thermal performance with a hot spot temperature about 6% to 14% lower than the others. The temperature of the hotspot remains around 70 ℃ with a heat flux of 625 W/cm^2. The non-uniform fin-enhanced microchannel- cooling technology appears to be a promising hotspot thermal management approach under moderate background heat flux. In addition to the cooling performance, the pressure drop should be considered for all the chips. Pressure drop of hydrofoil spanwise chip is highest among all the case, however, the pressure drop difference compared to others decrease from 44% to 20% with higher flow rate.

CHAPTER 3. PIN-FIN-ENHANCED MICROFLUDIC COOLING MANIFOLD FOR 2.5D-SICS

In this chapter, a micro-channel dielectric coolant manifold for 2.5D-SICs with multiple high-power dies, has been investigated for avionic cooling application. As mentioned in the previous chapters, 2.5D-SICs with higher data transmission speed and better signal quality, however, it requires unique and advanced cooling management method to provide non-uniform and enhanced cooling capacities for their heterogeneous dies. Limited studies addressed the thermal challenge with high-heat flux heterogeneous dies in 2.5D-SICs. More thermal challenges appear with the aircraft application of these 2.5D-SICs because of limited space, harsh working conditions such as high inlet coolant temperatures, and dielectric coolant requirement. To address the avionic cooling challenges and enable the aircraft application of 2.5D-SICs, a heterogeneous pin-fin enhanced cooling manifold with dielectric coolant has been designed and studied. To provide non-uniform and enhanced cooling capacity, thermal and hydraulic performance of chip placement, dimensions of micro-fin-bridges and micro-pins, and dielectric coolant supply and removal locations in the manifold have been parametrically studied by full-scale computational fluid mechanics/heat transfer simulations.

3.1 2.5D-SIC Model

The FPGA die is 25 mm × 25 mm, and the four transceivers are 6 mm × 6 mm each. The FPGA is placed between two pairs of transceivers. Five chip arrangements, seen in

Fig. 16 have been considered. There are two 1 mm gaps filled with a dielectric coolant between FPGA, and two pairs of transceivers to achieve hot spots thermal isolation.

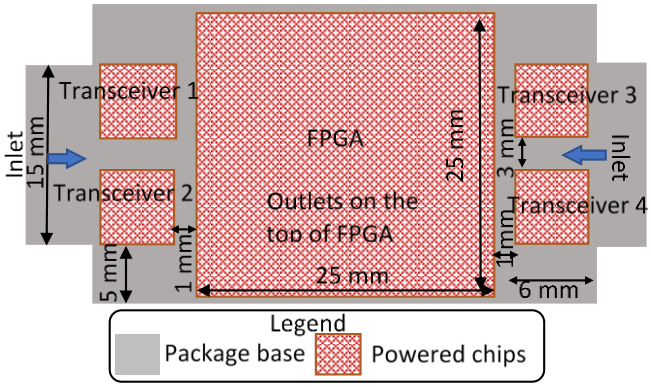


Figure 16: Locations of heaters with the package.

Pin-fin enhanced liquid cooling manifold with two inlets at the sides in Fig. 17, has been placed on top of all heaters of height 0.6 mm. Of these four transceivers, each pair is upstream of the FPGA for one inlet. One outlet of the manifold has been placed on top of the FPGA. Silicon pin-fins of height 0.6 mm are directly placed on top of five heaters within the manifold. The manifold design has been shown in Fig. 17, with cross sectional view at the center of one transceiver, top view at the half height of the inlet (as well as half height of fins), and top view at the half height of chips. To provide enhanced cooling capacity to this heterogeneous 2.5D-SICs configuration, micro-fin enhanced silicon bridges and wings have been implemented in the manifold. Each pair of transceivers is connected by a silicon bridge, shown in gray in Fig. 17 (c). Similar to transceivers, 0.6 mm high silicon fins are on top of the bridge. Silicon wings are the extended structures connected to each pair of transceivers with the same width as transceivers, and 0.6 mm height straight silicon fins are on top of the wings.

To enable the parametric study, various models were built with the commercially available ANSYS Icepak 16.2, that uses FLUENT 16.2 solver [54]. The computational fluid dynamics and heat transfer (CFD/HT) solver is based on finite control volumes. Each full-scale simulation model with 3 million nodes, includes inlets, outlets, and a micro-gap with five heaters and their cold plates in a package. Multi-level meshing with increased mesh is performed in the micro-gap, including pin-fin structures. Mesh independence study is performed. For the boundary conditions: Uniform constant velocity at 5.4 cm^3/s, and temperature at 55 ºC of coolant PAO (Polyalphaolefin) is applied for both inlets; free flow outlets with the laminar flow condition; radiation is included in the model; ambient temperature is 55 ºC; Five conducting silicon chips with thickness of 0.6 mm that located on the package of FR-4 have volumetric power. Governing equations of fluidic mass, momentum and energy conservation are:

$$\frac{\partial u}{\partial x}+\frac{\partial v}{\partial y}+\frac{\partial w}{\partial z}=0 \tag{2}$$

$$\rho\left(u\frac{\partial u}{\partial x}+v\frac{\partial u}{\partial y}+w\frac{\partial u}{\partial z}\right)=-\frac{\partial P}{\partial x}+\mu\nabla^2 u \tag{3}$$

$$\rho\left(u\frac{\partial v}{\partial x}+v\frac{\partial v}{\partial y}+w\frac{\partial v}{\partial z}\right)=-\frac{\partial P}{\partial y}+\mu\nabla^2 v \tag{4}$$

$$\rho\left(u\frac{\partial w}{\partial x}+v\frac{\partial w}{\partial y}+w\frac{\partial w}{\partial z}\right)=-\frac{\partial P}{\partial z}+\mu\nabla^2 w \tag{5}$$

$$\rho c_p\left(u\frac{\partial T}{\partial x}+v\frac{\partial T}{\partial y}+w\frac{\partial T}{\partial z}\right)=k\nabla^2 T \tag{6}$$

The thermal diffusion equation in the silicon solid domain is:

$$\frac{\partial}{\partial x}\left(k_{si}\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k_{si}\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k_{si}\frac{\partial T}{\partial z}\right)=0 \tag{7}$$

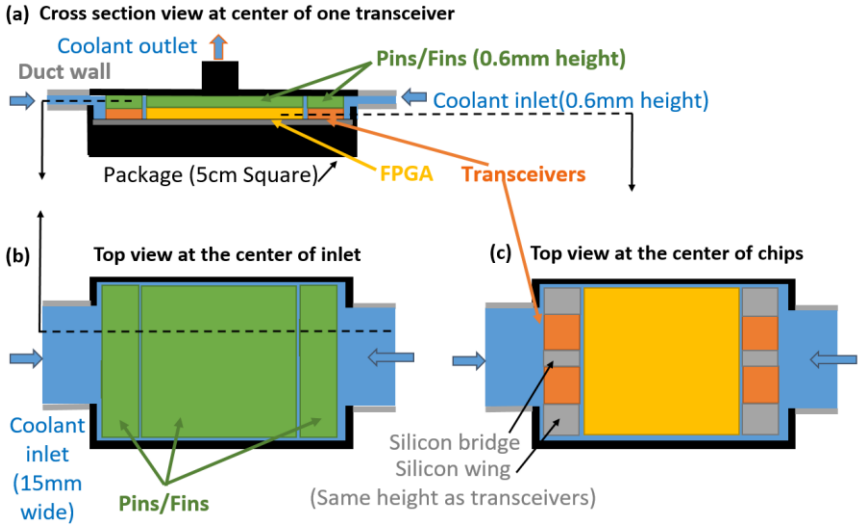


Figure 17: Manifold design for 2.5D-SICs.

3.2 Parametric Study of 2.5D-SIC Cooling Manifold

In this section, simulation results of chip temperatures and manifold pressure drops for parametric study of manifold characteristics are presented. These selected characteristics of this 2.5D-SIC cooling manifold are bridge-wing structure configurations, transceiver fin configurations, FPGA pin configuration and outlet configurations.

Mesh independent test has been performed as shown in Table 6 from both thermal and hydraulic perspectives. Compared with other cases, mesh case 2 with 3.74 million nodes are elected, as maximum temperatures, center location temperature, pressure drop and velocity are relatively stable with lower grid resource consuming.

Table 6: Mesh independent study.

Mesh Cases	1	2 (Chosen)	3	4
Nodes Numbers	2.96 Million	3.74 Million	3.98 Million	7.54 Million
Max Temperature of FPGA (ºC)	86.3	85.3	85.4	84.9
Temperature at FPGA Center (ºC)	85.0	84.0	83.6	83.2
Max Temperatures of Transceivers (ºC)	89.1	89.0	90.2	89.3
Temperatures at Transceiver Center (ºC)	88.4	88.6	89.8	88.9
Pressure Drop (N/m^2)	44647	45880	45600	46064
Average Coolant Velocity on the Top of FPGA (m/s)	3.0	3.2	3.2	3.3

3.2.1 Cooling Enhancement of Bridge and Wing Structures

Cooling performance of micro-fin enhanced silicon bridges and wings has been studied with the same power map and flow rate of 5.4 cm^3/s, as shown in Fig. 18. PAO (Polyalphaolefin), a dielectric coolant employed in avionics applications has been employed. Coolant at 55 ºC is pumped into both manifolds from two inlets on both sides, and discharged through two square outlets of 6 mm×6 mm at the top of the FPGA. In the cooling manifold without silicon bridge and wings, shown as Fig. 18 (a), straight fins of thickness 0.18 mm and pitch 0.18 mm are directly located on four transceivers. Cylindrical pins of radius 0.2 mm and pitch 1.8 mm are located on the FPGA. Fig. 18 (a) shows the temperature field of five heaters. Maximum temperatures of four transceivers reach 179.6

ºC. Pressure drop is 4850 N/m^2. In contrast, by implementing silicon bridge-wing structures with straight fins of the same dimension as on transceivers, temperatures of transceivers are significantly reduced to 105 ºC, indicated in Fig. 18 (b). Although the transceiver temperatures are still higher than the desired 85 ºC and pressure drop increases to 19,937 N/m^2, the cooling enhancement has been demonstrated. The transceiver temperatures could be further alleviated by optimizing the fin structures on the transceivers, and the FPGA, and inlet and outlet arrangements.

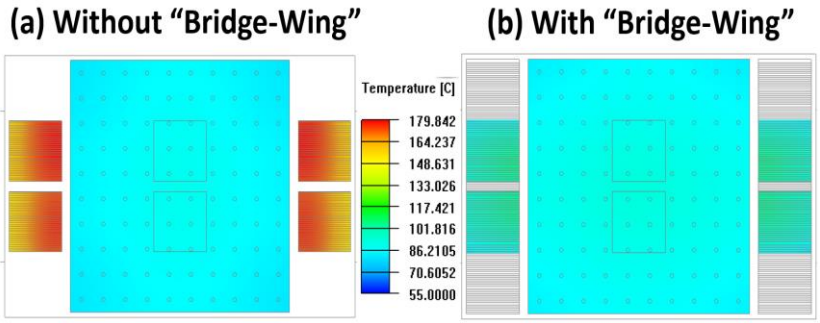


Figure 18: Cooling enhancement of bridge-wing structure: (a) Manifold without the bridge-wing structure (b) Manifold with the bridge-wing structure.

3.2.2 Fins on Transceivers

Cooling performance of micro-fin structures on transceivers and silicon bridges and wings has been studied with the same power map and flow rate of PAO at 5.4 cm^3/s, and inlet temperature of 55 ºC. Cylindrical pins of radius 0.2 mm and pitch 1.8 mm are located on FPGA for all the tested cases in Table 5. Six tested cases for straight fin configurations with both fin thickness and fin pitch from 0.11 to 0.18 mm have been simulated in full-scale computational fluid dynamics and heat transfer (CFD/HT). Due to the cooling manifold thickness limitation in this study, fin height is fixed at 0.6 mm that is as thick as FPGA and transceivers. Maximum temperatures of transceivers and FPGA, and pressure

drop have been listed in Table 7. As can be seen from the table, temperatures of transceivers are decreasing from case 1 to 6 with thinner fins and pitches. Case 6 with a straight fin thickness and pitch of 0.1 mm has the lowest temperatures at 89.3 ºC. It is observed that temperatures of transceivers show decreasing improvement from case 1 to 6, and temperatures between case 5 and 6 are relatively close with temperature difference of 0.4 ºC. Even if pin configurations on the FPGA are the same for all cases, FPGA temperatures keep increasing from case 1 to 6. This phenomenon could be caused by higher coolant temperatures after transceivers, as fins on transceivers of case 6 have enhanced cooling performance. Pin configuration studies will be reported in the next section. Pressure drop increases from case 1 to case 6 because of denser fins on transceivers.

Table 7: Simulated cases of various fin configurations on transceivers.

Model No.	1	2	3	4	5	6
FT (mm)	0.18	0.15	0.14	0.12	0.11	0.1
FP (mm)	0.18	0.15	0.14	0.12	0.11	0.1
Number of Fins	69	83	89	104	113	125
Max T_{tr} (ºC)	101.4	96.2	96.2	90.9	89.7	89.3
Max T of FPGA (ºC)	92.8	93.0	93.0	93.1	93.3	93.9
ΔP (kN/m^2)	19.9	23.4	23.4	28.3	30.9	32.0

3.2.3 Pins on FPGA

Cooling performance of micro-pin structures on the FPGA has been studied with the fin configurations in case 6 listed in Table 7, and same power map and flow rate of PAO at 5.4 cm^3/s, 55 ºC inlet temperature. Straight fins with both fin thickness and pitch 0.11 mm are adopted on transceivers and silicon bridges and wings for all the tested cases in Table 8. Six tested cases for cylindrical pin configurations of radius 0.12, 0.2 and 0.25 mm, and pitch 2 to 2.4 mm have been simulated in full-scale CFD/HT. Half of the tested cases have 100 pins, and the other half have 144 pins. Maximum temperatures of transceivers and the FPGA, and pressure drops have been summarized in Table 8. As seen from Table 8, temperatures of FPGA with 100 pins are in the range of 88.3 ºC to 91.2 ºC, which is higher than temperatures of FPGA with 144 pins in the range of 85.3 ºC to 88.8 ºC. For the three cases with 144 pins, case 12 with largest radius has the lowest FPGA temperature at 85.3 ºC. In contrast to the fin optimization in the previous section, various pin configurations on the FPGA have a minor effect on transceivers, with temperatures around 88.9 ºC, as the FPGA is located downstream of the transceivers. However, pressure drops are affected by pin configurations. Pressure drops in three cases of 144 pins are in the range of 43.1 to 45.9 kN/m^2, which is higher than other three cases of 100 pins in the range of 42.6 to 43.9 kN/m^2. For each of the three cases in the group with same number of pins, pressure drop increases with larger pin radius. This phenomenon could be caused by the smaller pitch between pins with a larger radius.

Table 8: Simulated cases of various pin configurations on the FPGA.

Model No.	7	8	9	10	11	12
Pins	100	144	100	144	100	144
Pin Radius (mm)	0.12	0.12	0.2	0.2	0.25	0.25
Pin Pitch (mm)	2.4	2.1	2.3	2.05	2.2	2
Max T_{tr} (ºC)	89.0	88.6	89.1	89.2	88.9	88.8
Max T of FPGA (ºC)	91.2	88.8	89.2	86.4	88.3	85.3
ΔP (kN/m^2)	42.6	43.1	43.3	44.7	43.9	45.9

3.2.4 Outlets Configurations

Studied outlet configurations in this section include: location, numbers and areas. Location optimization is mentioned in 3.2.4.1, and numbers and areas are presented in the section of 3.2.4.2.

3.2.4.1 Outlets Locations.

The cooling performance of two outlet location above the FPGA has been studied with the fin configurations in case 6 in Table 7, and pin configurations in case 12 in Table 8. Constant power map and flow rate of PAO at 5.4 cm^3/s, 55 ºC are adopted in the CFD/HT simulations.

Temperature fields and flow velocity fields from CFD/HT simulations with two outlet locations are shown in Fig. 19. Fig. 19 (a) has simulation results of the case with the locations of two outlets at the sides of the FPGA. As can be seen from both temperature field and velocity vectors, temperatures are higher in the center of the FPGA, as most of coolant would directly flow to both outlets without flow above the center of the FPGA. The maximum temperature of all dies is 99.3 ºC at the center of the FPGA. All transceivers are lower than 90 ºC. Fig. 19 (b) has simulation results of the case with the locations of two outlets in the center of the FPGA. Compared to previous case in Fig. 19 (a), the temperature filed of this case is more uniform with maximum temperature 93.9 ºC at the center of the FPGA, which is lower than that of previous case. All transceivers are lower than 90 ºC. It is obviously seen that liquid cooling manifold with outlets above the center of the FPGA would contribute to the same temperatures of transceivers, but lower temperatures of the FPGA.

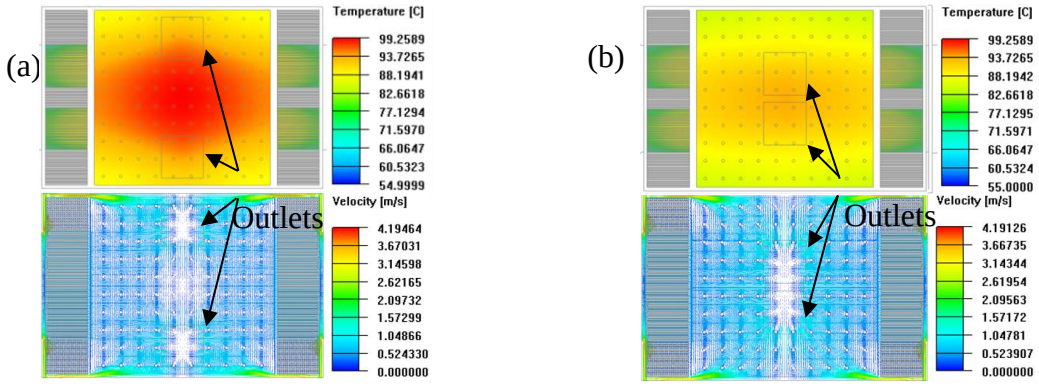


Figure 19: Temperature fields and flow velocity fields of two outlet locations: (a) Two outlets at sides (b) Two outlets in center.

3.2.4.2 Numbers and Areas of Outlets.

With the outlet located above the center of FPGA, outlets numbers and area have been investigated. Table 9 shows the CFD/HT simulation results for various outlet configurations with the same manifold pin-fin design in the prior section. Case 13 has the largest outlet areas and the highest FPGA temperature, in contrast to case 15. The temperatures of all transceivers are less affected by outlet arrangements. However, pressure drops are closely related to outlet areas. Case 15 with the smallest outlet area has the lowest FPGA temperature and highest pressure drop, because of the longer coolant cooling path on the FPGA.

Table 9: Simulated cases of various outlet configurations.

Model No.	13	14	15
Outlets	2	1	1
Outlet Area (Each)	6 x 6 mm	6 x 6 mm	2 x 2 mm
Max T of Transceivers (ºC)	89.3	89.3	89.1
Max T of FPGA (ºC)	93.9	90.4	89.2
Pressure Drop (N/m^2)	32031	33084	43343

Last but not least, in addition to these five studied characteristics, fins, instead of pins, have been selected and designed on top of the bridge-wing structures and transceivers

have been justified. Pins cooling performance on top of the bridge-wing structures and transceivers have been simulated under the same conditions of model 15. Temperature field and flow velocity vector field have been shown in Fig. 20 for two cases with various pin densities. The temperatures of all these two cases along with our selected fin structures of model 15 are presented in Table 10. As can be seen from Fig. 20 and Table 10, transceiver temperatures of model 16 and 17 with pins on top of transceivers are 10 ºC higher than that of model 15 with straight fins on top of transceivers, even if model 16 and 17 have very dense pin arrays. Thus, fin structures on top of transceivers and bridge-wing structures have been proven to achieve better cooling capacity and have been selected in the liquid cooling manifold.

(a) 264 Pins at upstream instead of fins (b) 450 Pins at upstream instead of fins

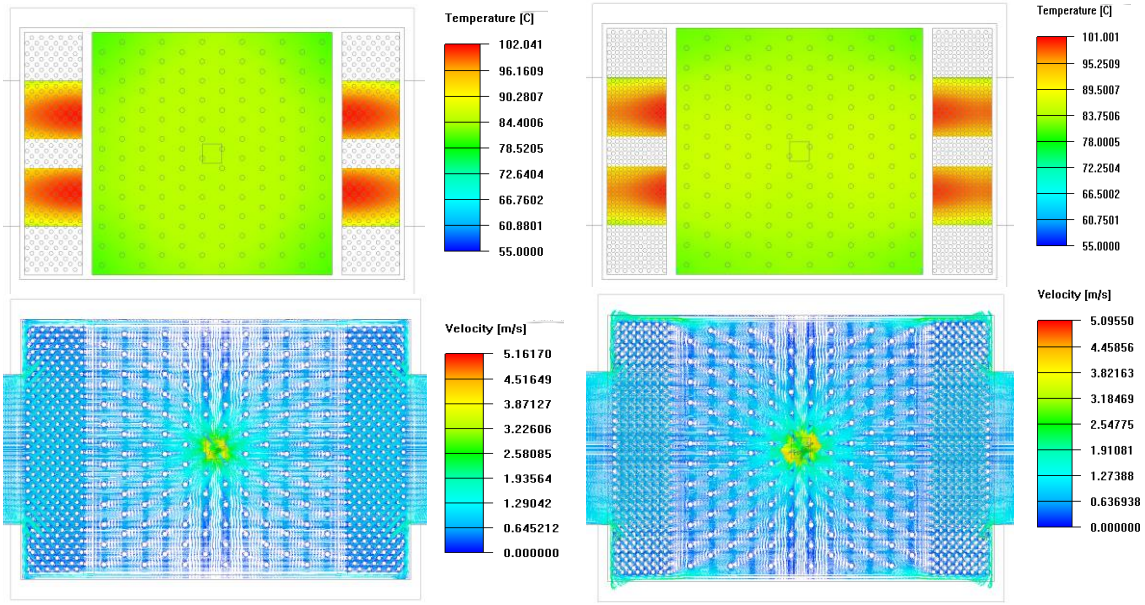


Figure 20: Temperature fields and flow velocity vector fields of two transceivers with various pin densities cases.

Table 10: Cooling performance of the models with Pins or fins on top of transceivers and bridge-wing structures.

	16	17	15
Enhancement on bridge-wing structures and transceivers	264 Pins	450 Pins	Straight Fins
Max T of Transceivers (ºC)	102.0	101.0	89.1
Max T of FPGA (ºC)	85.1	85.7	89.2
Pressure Drop (N/m^2)	21988	28724	43343

3.3 Optimized Configurations

Considering all the simulation results mentioned in the prior sections, the optimized manifold configurations are listed in Table 11. Constant power map and flow rate of PAO at 5.4 cm^3/s, 55 ºC have been adopted in the CFD/HT simulation. A simulation model with 3.7 million nodes can be seen in Fig. 21. Temperature fields of the simulation based on optimized configurations in the Table 11 are shown in Fig. 21. Maximum temperatures of the transceiver are 88.8 ºC and the FPGA 85.3 ºC, and pressure drop are listed in Table 11. Transceivers have the highest temperatures among all the dies, due to their high heat fluxes which pose challenges for dielectric liquid cooling. In addition to meeting the thermal management challenges of high power transceivers, this liquid cooling manifold with 1 mm micro-gaps between transceivers and the FPGA successfully solves the thermal coupling issues between heterogenous chips, by implementing liquid thermal isolation.

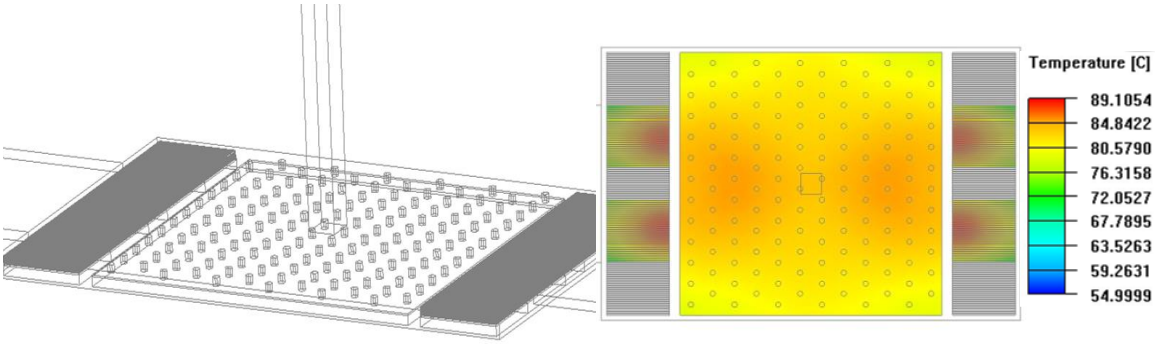


Figure 21: Optimized dielectric liquid cooling manifold and its temperature fields of heaters.

Table 11: Dielectric liquid cooling manifold configurations and their performance.

	Manifold Configurations		Max Temperatures	Pressure Drop
Fins on Transceivers	Fin Thickness	0.1 (mm)	89.1 (ºC)	45880 (N/m^2)
	Fin Pitch	0.1 (mm)		
Pins on FPGA	Pin Radius	0.25 (mm)	85.3 (ºC)	
	Pin Pitch	2 (mm)		
Outlets	Amount & Location	1 at center	N/A	
	Area	2 x 2 mm		

3.4 Summary

To meet the thermal challenges of 2.5D-SIC, a liquid cooling manifold with unique inlet and outlet arrangement, and special fin enhanced “bridge-wings” structures inside the manifold has been designed and optimized through parametric study in chapter three.

Each higher power density transceiver (30W, 6 mm x 6 mm) is cooled by PAO through a specified inlet. Silicon fin enhanced “bridge-wings” structures are designed between each pair of transceivers as the bridge, and also extend these transceivers as wings to enhance the cooling performance.

Fins on these “bridge-wings” structures and transceivers have been optimized to achieve cooling efficiency, with satisfactory cooling performance, and acceptable pressure drop. Cylindrical pins, instead of straight fins on FPGA have been designed and optimized to achieve an acceptable pressure drop. Flow direction guiding fins on the FPGA do not provide better cooling enhancement. 1 mm wide coolant filled micro-gaps between transceivers and FPGA contribute to enough thermal insulation between them, which protect the lower power FPGA from affecting by the high-power transceivers. Numbers, configurations and the location of outlet above the FPGA have been optimized for lower temperatures of FPGA and transceivers. With the optimized manifold configuration, including “bridge-wings” structures, temperatures of all five chips are lower than 90 ºC, even if thermal properties of dielectric coolant are only a third of these of water.

CHAPTER 4. OPTIMIZATION OF PIN-FIN CONFIGURATIONS IN MICRO-GAP LIQUID COOLING FOR 2.5D-SICS

In this chapter, non-uniform pin-fin structures for five chips in the micro-gap were systematically optimized by utilizing design of experiment (DoE) with full-scale computational fluid dynamics/heat transfer (CFD/HT) simulations. In contrast to the parametric study of cooling manifold with specially designed bridge-wing structures and inlets and outlets in the previous chapter, this chapter focus on optimization of heterogeneous pin-fin enhanced cold plate with one inlet at the side and one outlet on the opposite side. Thus, two high heat flux transceivers are located at the upstream and other two are located at the downstream. To provide non-uniform cooling capacities for all transceivers at both upstream and downstream and FPGA in the center, non-uniform heterogeneous pin-fin structures have been designed in the micro-gap of a cold plate on top of these heterogeneous dies. As the cold plate is one hydraulic system with heterogeneous pin-fin structures, pin-fin structures at upstream and downstream are related and affect each other. Thus, these pin-fin structures in upstream and downstream need to be systematically optimized to achieve the optimized and non-uniform cooling performance. In this chapter, design of experiment (DoE) coupling with CFD/HT has been investigated and applied in these multi-component-system optimizations for 2.5D-SICs. Optimized heterogeneous pin fin structures in the micro-gap of the cold plate for the 2.5D-SIC with five heterogeneous dies have been efficiently derived.

4.1 Cold Plate Designs for 2.5D-SICs

Five silicon chips, including four transceivers and one field-programmable gate array (FPGA), are located on top of a FR-4 package base with a thickness of 0.0014 m. All silicon heaters have the same thickness of 0.0006 m. Each of the four transceivers is 0.006 m × 0.006 m with uniform power of 30 W. The FPGA is 0.025 m × 0.025 m with total power of 100 W. A silicon cold plate with two pin-fin sections has been placed on top of five chips. Deionized water as coolant at 55 ºC is pumped through the cold plate via one rectangular inlet of the cold plate with dimensions of 0.015 m × 0.0015 m at a constant flow rate of 20 L/hr. One outlet on the opposite side of the package has the same dimensions. Transceivers 1 and 2 at the upstream and the FPGA are cooled by straight fins in the cold plate. In contrast, Transceiver 3 and 4 downstream are cooled by cylindrical pins. Both pin-fin structures from upstream to downstream should be systematically optimized.

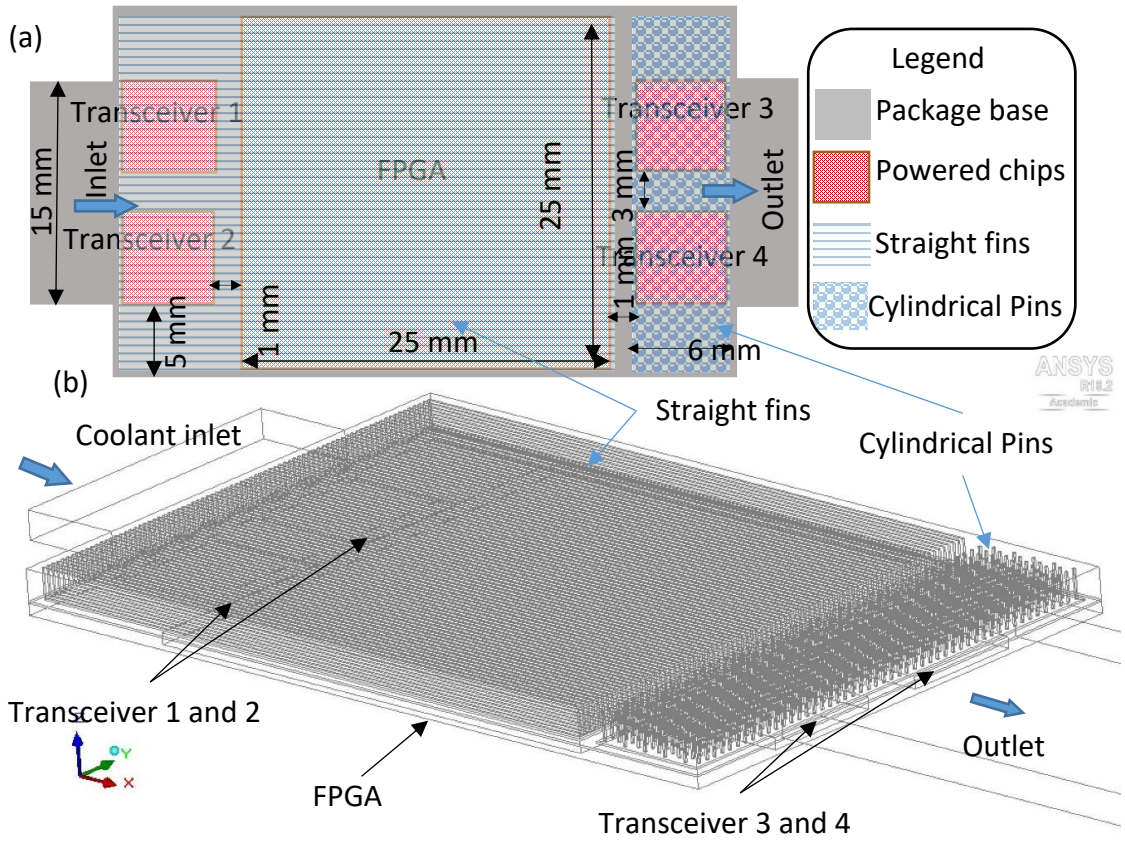


Figure 22: (a) Top view of heaters with cold plates; (b) 3D view of the model in CFD/HT.

4.2 DoE Methodology

Trial and error for optimizing experiments and products with various factors is time consuming and costly. In contrast, DoE, a statistic method, can cost-effectively characterize, predict, and eventually improve systems or designs [55]. The process of DoE is reasonable arranging experiments by identifying characteristics of related factors, then doing experiments with suggested factor characteristics and proposing an optimized design at the end based on limited experimental results [56-57]. Thus, optimized factors can be achieved with limited experimental tests to save time and cost. More importantly, for a complicated system design with multiple factors in this paper, an optimized configuration

is hard to achieve by doing trial and error. A postulated model is the basic mathematical theory behind the DoE, which is shown as equation 8:

$$y = a_0 + \sum a_i x_i + \sum a_{ij} x_i x_j + \sum a_{ii} x_i^2 + \cdots \quad (8)$$

where y is the response or interest, x_i represents a level of factor i, x_j represents a level of factor j, and a_0, a_i, a_{ij}, a_{ii} are the coefficients of the polynomial. For various conditions x and the corresponding y, various equations with various y, a, and x can be established. matrix $\hat{y}$ represents a matrix with all y, matrix $\hat{x}$ represents a matrix with all x, and $\hat{a}$ represents a matrix with all a which should be solved in equation 9:

$$\hat{a} = (\hat{x}'\hat{x})^{-1}\hat{x}'\hat{y} \quad (9)$$

where matrix $\hat{x}'$ is the transpose of the matrix $\hat{x}$, JMP and others, like SAS/STAT, can solve the matrix for $\hat{a}$. Then the importance of various factors x can be analyzed with known coefficients $\hat{a}$.

4.3 Results and Discussions

2.5D-SICs optimization processes of implementing the DoE method in conjunction with CFD/HT full scale simulations are introduced in this section, including target setting, parameter selections, DoE suggested representative cases supported by CFD/HT, and DoE suggested optimized parameters. Temperatures and pressure drop of this optimized 2.5D-SICs cold plate have met the design targets with CFD/HT verification.

4.3.1 Target Temperatures and Pressure Drop

Five parameters are used to optimize cold plate with both straight fins and cylindrical pins: ① Height of straight fin and cylindrical pins could be 0.5 mm, 1 mm, and 1.5 mm. ② Thickness of straight fins in a range of 0.1 to 0.12 mm. ③ Pitch of straight fins in a range of 0.1 to 0.3 mm. ④ The diameter of cylindrical pins in a range of 0.14 to 0.2 mm. ⑤Numbers of cylindrical pins in a range of 300 to 500.

Constraints/targets: all five chip temperatures are lower than 84 ºC and pressure drop is as low as possible.

4.3.2 Representative Cases with CFD/HT Model

	Height	Thickness	Pitch	D	Numbers
1	1.5	0.11	0.2	0.14	500
2	0.5	0.11	0.3	0.14	500
3	1.5	0.1	0.1	0.14	400
4	0.5	0.11	0.2	0.2	500
5	0.5	0.12	0.1	0.14	400
6	1	0.12	0.3	0.17	400
7	1.5	0.11	0.3	0.2	500
8	1	0.11	0.1	0.17	400
9	1.5	0.11	0.2	0.2	300
10	1	0.1	0.274	0.17	400
11	1.5	0.12	0.1	0.14	400
12	0.5	0.11	0.3	0.2	300
13	1.5	0.11	0.3	0.14	300
14	0.5	0.1	0.1	0.14	400
15	0.5	0.11	0.2	0.14	300

Figure 23: JMP suggested cold plate configurations of 15 representative cases for CFD/HT simulations.

Based on related parameter settings, JMP suggests cold plate configurations of 15 representative testing cases with various parameters, shown as Fig. 23. All these suggested models are performed in CFD/HT, ANSYS Icepak 16.2, that uses FLUENT 16.2 solver [54]. This computational fluid dynamics and heat transfer (CFD/HT) solver is based on finite control volumes. Governing equations of fluidic mass, momentum and energy conservation, and thermal diffusion equation in the silicon solid domain are Equ. 2 to 7.

Table 12： Mesh independence study for case 1 configuration with 4 mesh sizes.

Mesh Samples	1	2	3 (Chosen)	4
Nodes Numbers	3667290	4452437	4496405	4913656
Temperature of FPGA (ºC)	69.7	69.6	69.6	69.6
Temperature at FPGA Center (ºC)	62.5	62.5	62.5	62.6
Temperatures of Transceiver 1 and 2 (ºC)	70.0	70.1	70.1	70.2
Temperatures at Transceiver 1 and 2 Center (ºC)	69.3	69.5	69.5	69.5
Temperatures of Transceiver 3 and 4 (ºC)	92.2	91.6	91.5	91.5
Temperatures at Transceiver 3 and 4 Center (ºC)	87.7	86.8	86.8	86.7
Pressure Drop (N/m^2)	1682	1700.0	1699.0	1684

Meshes of models vary from 3.5 to 5 million in all these cases, with same mesh size of 0.0001 m in x, y and z direction, because of various cold plate designs. Mesh independence has been verified, as summarized in Table 12 with four different mesh sizes for the first representative testing cases with JMP suggested parameters. In this table, the node numbers increase from mesh sample 1 to 4, and the temperatures of all chips become stable after sample 2. Thus, temperature results are not dependent on the node numbers when the mesh nodes exceed 4.4 million. The mesh size in mesh sample 3 has been chosen for all other 14 cases. 15 CFD/HT models are built and simulated in ANASYS Icapak individually with their suggested pin-fin configurations. Temperatures of two transceivers at upstream, an FPGA in the middle, and two transceivers at downstream are acquired and listed in Table 10. Pressure drops of all these cases are also presented in Table 13.

4.3.3 Optimized Cold Plate Structures with CFD/HT Model

Analyzing all these results, JMP suggests a set of optimized configurations: pin and fin height of 1 mm, thickness of straight fins as 0.11 mm, pitch of straight fins as 0.2 mm, and 500 cylindrical pins with a diameter of 0.2 mm, as shown in Fig. 23. Optimized temperatures and pressure drop are acquired by running a CFD/HT model with suggested configurations, and listed in table 11. The temperature field of chips with optimized cold plate configurations has been shown in Fig. 24. As can be seen from the optimized results, all temperatures meet requirements and pressure drop is minimized, as all the 15 modeled cases with satisfied temperatures have higher pressure drops.

Table 13： Simulation results for all 15 cases.

Simulation Cases	Temperatures of Transceiver 1 and 2 (ºC)	Temperature of FPGA (ºC)	Temperatures of Transceiver 3 and 4 (ºC)	Pressure Drop (N/m^2)
1	70.1	69.6	91.5	1700.0
2	75.2	74.4	83.6	4824.1
3	67.6	70.5	97.9	4841.0
4	72.1	70.0	79.7	8691.3
5	67.8	68.5	88.0	21672.3
6	70.4	68.9	82.1	3143.3
7	73.8	71.7	84.4	1047.0
8	67.0	69.7	89.9	8494.2
9	70.5	69.5	91.2	1595.6
10	73.0	71.8	86.7	1729.0
11	67.5	70.6	98.1	5444.0
12	75.2	74.6	86.3	4389.4
13	74.2	73.7	98.7	778.5
14	67.5	68.5	87.8	20159.1
15	72.1	70.7	89.0	6858.0

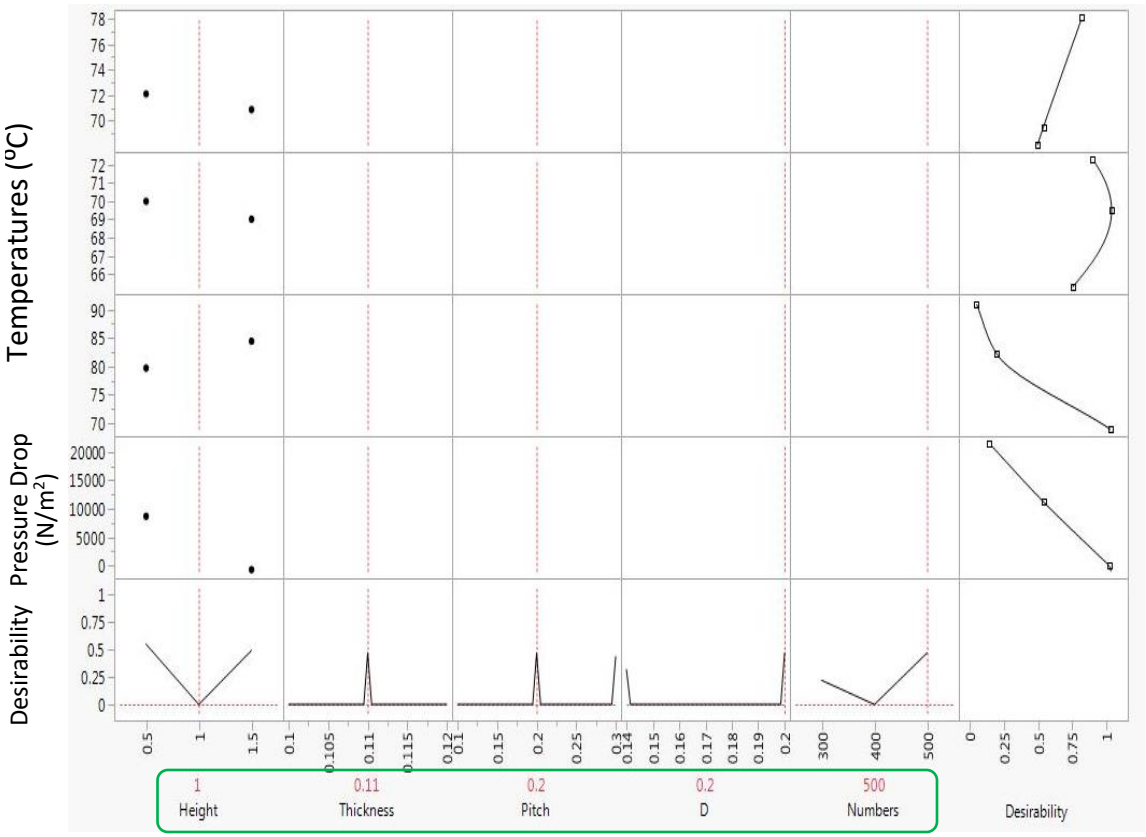


Figure 24： Optimized cold plate configurations for CFD/HT simulations.

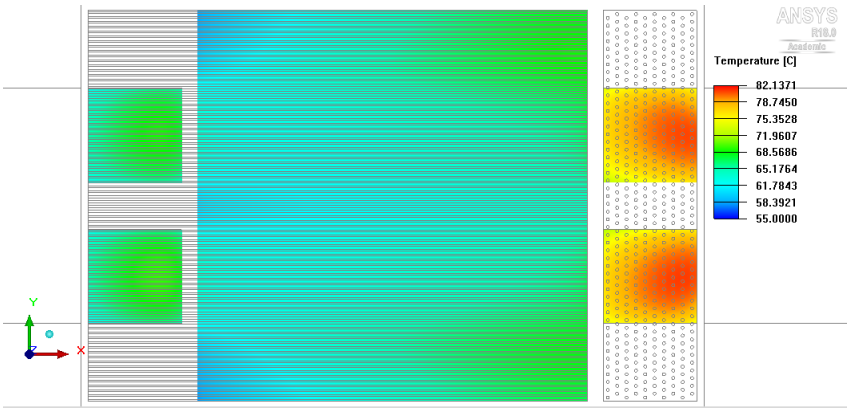


Figure 25： Temperature field of chips with optimized cold plate configurations from CFD/HT simulations.

Table 14： Heater temperatures and pressure drop of CFD model with optimized configurations.

Optimized Configurations	Height of Pins and Fins (mm)	Thickness of Straight Fins (mm)	Pitch of straight fins (mm)	Number of cylindrical pins	Diameter of cylindrical pins (mm)
	1	0.11	0.2	500	0.2
Optimized Results	Temperatures of Transceiver 1 and 2 (ºC)	T of FPGA (ºC)	Temperatures of Transceiver 3 and 4 (ºC)	Pressure Drop (N/m^2)	
	70.3	68.9	82.1	3138	

For the optimized result, it suggests very dense pin arrays with larger pin diameters for the downstream cold plate to keep the temperatures of transceivers 3 and 4 in our target range, but proper fin density for the upstream heat sink to achieve targeted temperatures as well as a lower pressure drop for entire flow. Modest channel height (pin fin height) with 1 mm has been selected as optimum configuration, instead of higher pins to increase the pin areas.

4.4 Summary

In chapter four, a cold plate with heterogeneous pin-fin structures have been systematically optimized for a 2.5D-SIC with five heterogeneous chips by using both DoE with CFD/HT.

Same as already commercialized cold plates, this 2.5D-SIC cold plate has one inlet on one side and one outlet on the other side. Uniform pin or fin structures would not overcome the thermal challenges of 2.5-SICs, due to their chip arrangements: high power density chips are located at both upstream and downstream. Heterogeneous pin-fin structures should be adopted to achieve the similar cooling capacity for all upstream and downstream chips. These pin-fin structures should be optimized systematically as over enhanced pin structures on the downstream chips would lead to higher temperatures of upstream heaters, as well as a high pressure drop for this cold plate.

All characteristics of heterogeneous pin-fin structures have been systematically optimized by DoE and CFD/HT in the selected range, including: height, thickness, and pitch of straight fins on the top of the upstream chips and an FPGA; height, diameter, pitch of cylindrical pins on the top of the downstream chips. Providing full scale CFD/HT simulation results of all cases to JMP, a DOE software, ensures the optimized targets (temperature and pressure drop restrictions) in the selected characteristic ranges. Provided and verified by CFD/HT, the cold plate design with optimized pin-fin configurations has met the targets: all temperatures are lower than 84 ºC and pressure drop is as low as possible.

CHAPTER 5. COMPACT THERMAL-ELECTRICAL CO-DESIGN MODEL FOR 3D-SICS

In addition to the previous chapters focus on liquid cooling thermal management for 2.5D-SICs, a compact thermal-electrical co-design simulation model for 3D-SICs with pin-fin enhanced micro-gaps is presented in this chapter. Similarly, to 2.5D-SICs, 3D-SICs suffer from thermal challenges because of stacked heterogeneous dies which are connected by TSVs. Liquid cooling performance in the micro-gap between dies with pin-fin type TSVs have been simulated by others using CFD and porous media theory in the micro-gaps. These studies are either time and resource consuming or lack of analysis of physical pin-fin configuration. To address both problems from previous studies for rapid simulation with consideration of pin-fin physical structures as well as realistic leakage power, a model for both steady state and transient state, considers spatially and temporally varying heat flux distribution in each tier, and various coolant characteristics in each micro-gap has been built and presented in this chapter. Actual leakage estimation is included in this co-design model which contribute to co-designed actual temperature fields in 3D-SICs.

5.1 Compact Thermal Model

In this section, illustrations of a four- layer 3D-SIC with pin-fin enhanced micro-gaps are presented. In addition, as this co-design model has both thermal and electrical simulation functions, thermal analysis and the verification are presented in this section. Electrical analysis will be presented in the next section.

5.1.1 Model of 3D-SICs

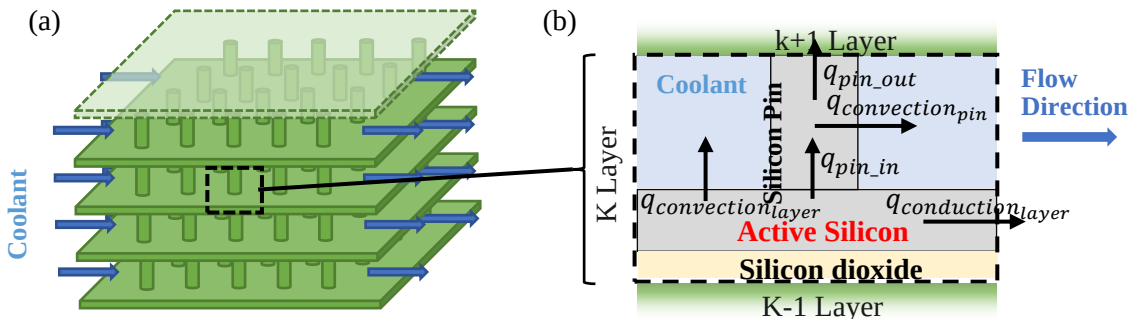


Figure 26: (a) Microfluidic cooling 3D-SIC model of four layers; and (b) energy equation analysis of control volume of a pin.

Fig. 26 (a) shows a schematic of a 3D-SIC micro-fluidic cooling model of four layers, each of which contains several components with different power. Generated by different power, heat is dissipated by a coolant that runs through the microchannel between layers connected by cylindrical pin-fins, which transfer both heat and electronic signals. This characteristic leads to enhanced cooling performance as well as electrical signal transfer because of an increase in the contact cooling surface and the amount of TSVs in each pin fin, respectively.

2.2 Thermal Analysis

The model is discretized into multiple identical control volumes, each around a single pin. Energy balance equations are built for each control volume. Fig. 26 (b) shows a thermal analysis of a control volume in the middle layer with a micro-gap. Each control volume block includes both solid components and liquid as a micro-gap. Solid components in each layer include an active silicon layer with heat generation, a silicon dioxide layer, and a silicon pin. Because of the various heat generation rates within each layer and pin-

fin- connected layers, the model considers both horizontal and vertical directions of heat conduction through control volumes. Besides conduction, the model includes forced convection heat transfer within control volume, which plays an important role in coolant-contacted surfaces of both layers and pin fins. Correlations of friction factor and Colburn j factor have been utilized to calculate heat transfer coefficient of forced convection and pressure drop. These correlations have been built by detailed CFD/HT simulations within the certain range (22< Re <357, 1.5< ratios of pitch to diameter <2.25, and 1.5< ratios of height to diameter <2.25), and have been validated [30-31]. In addition to the forced convection, the model has free convection from the 3D-SICs to the ambient. This model excludes radiation because of the negligible radiation heat transfer rate.

The energy equations of the layer and the coolant in Fig. 26 (b) are below. The energy equations of a coolant follow:

$$\dot{m} \cdot C_P \cdot \Delta T = q_{conv_{pinf}} + q_{conv_{layer}} \tag{10}$$

$$q_{conv_{pin}} = q_{pin\_in} - q_{pin\_out} \tag{11}$$

The energy equation of each layer follows:

$$q_{gen} = q_{pin\_in} + q_{conv_{layer}} \tag{12}$$

5.1.2 Verification of the Compact Model

A four-layer CFD/HT ANASYS model was built to validate the compact micro-fluidic cooling model. In Fig. 27 (a), the CFD/HT model, which simulates one stripe along

the way because of its symmetric structure, consists of the following parameters: the diameters of the pins are 100 μm, the transversal and longitudinal pitches are 110 and 220 μm. The inlet fluid and ambient temperature are 298K. For each of the four layers, the heating sources are 2.5×10^{10} W/m^3. The convection heat transfer coefficients are 550 for the bottom and 10 W/m^{2}K for the top surface of the model, and two side walls are symmetric. The dimensions of the layers and boundary conditions from the compact thermal model have been applied to the CFD/HT model with 3.5 million modes, which meets the requirement of mesh independence for reliable temperature results. The sweep meshing method has been adopted for four-layer pin-fin which enable higher quality meshing. The inflation meshing option has been adopted for Pin-fins liquid interface, and set as 6 maximum layers with the 1.1 growth rate. This meshing option increases meshes around the pin-fin to accurately calculate thermal transfer characteristics within boundary layers. The meshing performance of this inflation meshing option can be seen in partial enlargement of meshing on side view; Fig. 27 (c) shows that the maximum temperatures of these two models are closely agreed. In addition to its accuracy, the compact model is also efficient, taking less than one minute to acquire results. This calculation speed of the compact model is significantly faster than that of the CFD/HT model, which runs on a 2.5 GHz CPU and 8 GB memory desktop for around 20 hours.

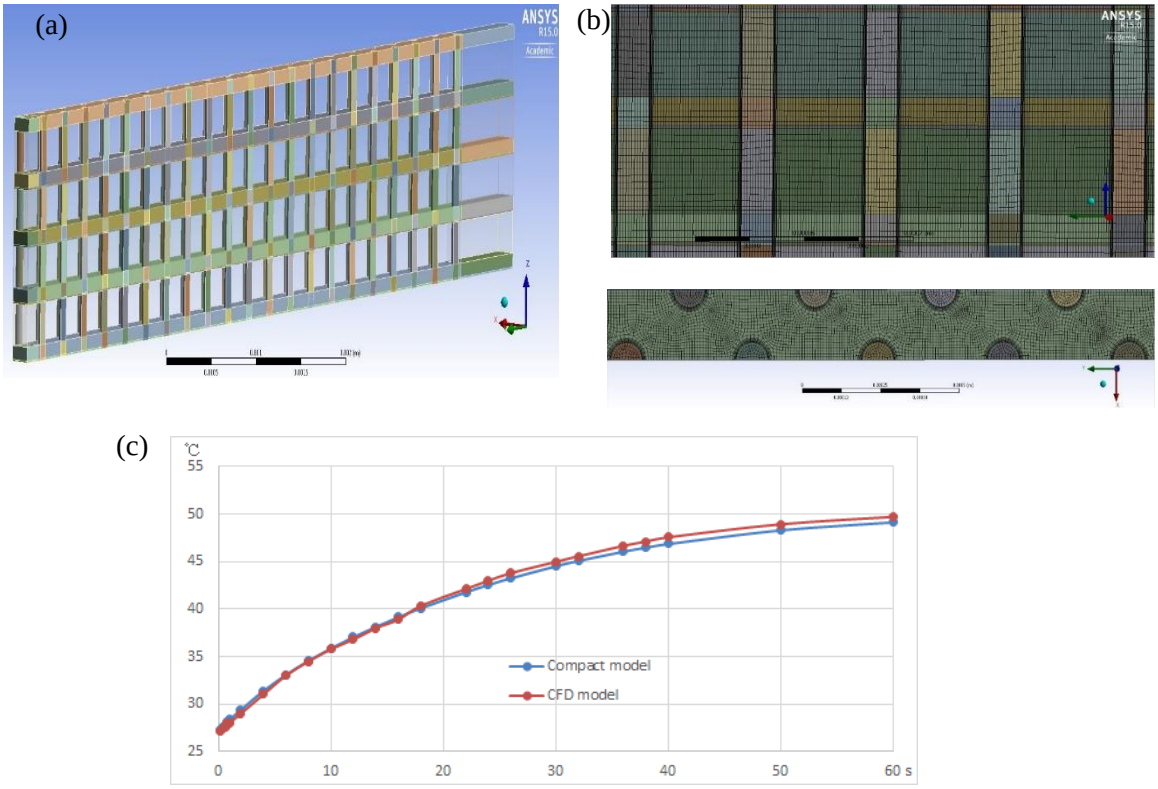


Figure 27: (a) Structure of the CFD/HT model; (b) partial enlargements of meshing on both side view and top view; (C) comparison of the maximum temperature of one layer between the CFD/HT and compact models.

5.2 Thermal-electrical co-design

In addition to the thermal simulation features of the compact model, actual electrical leakage prediction function has been adopted into this compact model. Implementing McPat power simulator, a Ph.D. student in electrical engineering department, Obaidul Hossen acquired the dynamic and leakage power ratio of the Penryn processor are 4:1, which means 80% of chip power are dynamic power and the other 20% are leakage power [58]. Leakage power of chips is correlated with their chip temperatures, as shown in Fig. 28 by implementing 45 nm HP model with 50 inverter circuits in HSPICE

[59]. The higher the temperature, the higher leakage power. The 20% leakage power is estimated based on the 100 ºC chip temperature, which contributes to over-estimated leakage power because of the lower chip working temperature. These over-estimated leakage power are calculated by implementing the chip temperatures that generated by the compact thermal model into the realistic power ratio and temperature correlation, as shown in Fig. 28 (b). Realistic power is acquired by deducting these over-estimated leakage power. Based on the actual updated power from the electrical perspective, actual chip temperatures have been further updated in the compact model that are closer to reality and only acquired by considering both thermal and electrical perspectives.

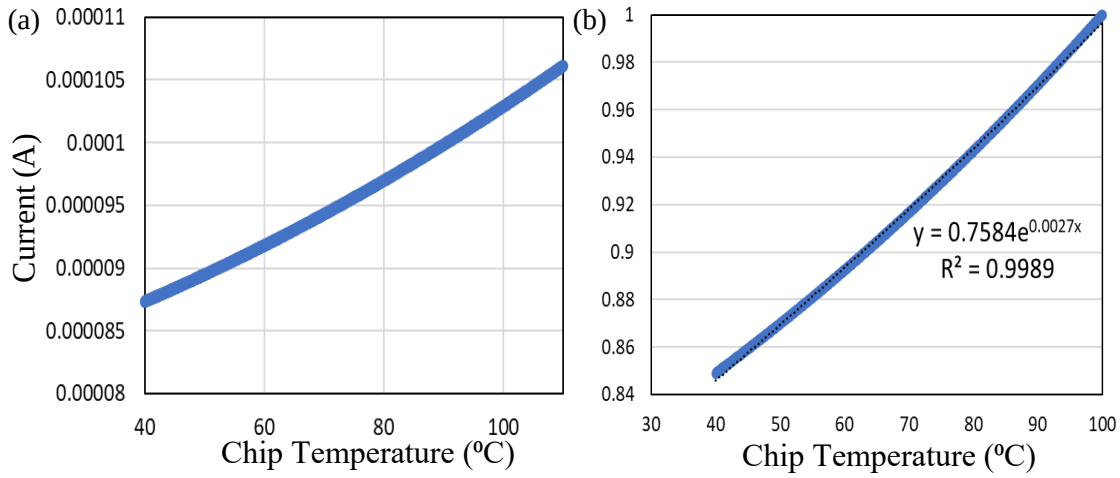


Figure 28: (a) Correlation of temperature vs. current leakage generated from HSPICE (b) realistic leakage power ratios with chip temperatures.

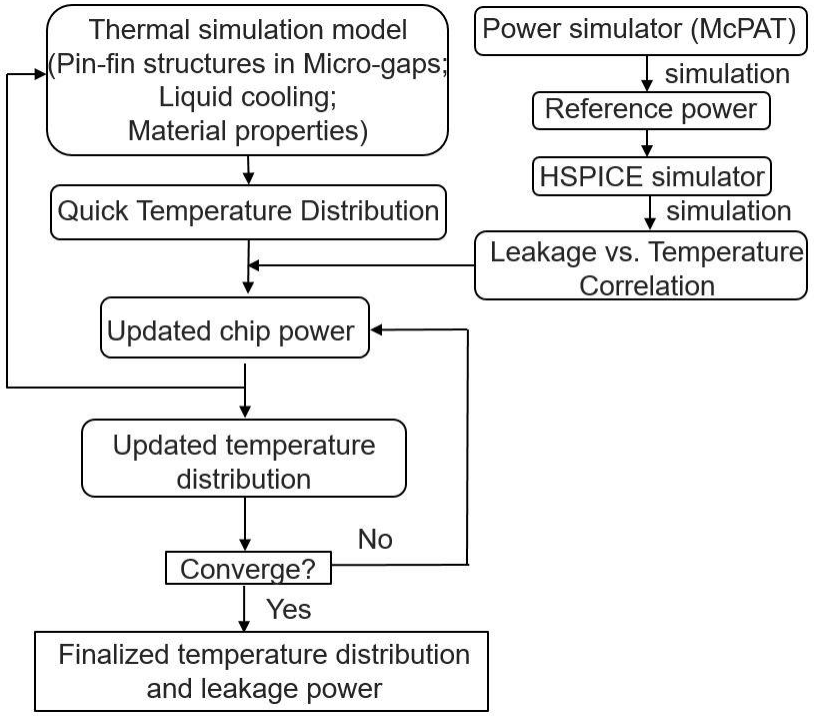


Figure 29: Flow-diagram of thermal-electrical co-design model.

5.3 Configurations and Power Maps of the Four Layers 3D-SICs Compact Model

In this section, configurations of a four- layer 3D-SIC with pin-fin enhanced micro-gaps are presented. These configurations include both layer and coolant configurations as well as applied power maps.

5.3.1 3D-SICs Layers Configurations

Configurations of 3D-SICs model with pin-fin enhanced micro-gaps are shown in Fig. 30. It is a four active layer model. These four layers are identical with a width of 1.6×10^{-2} m, length of 1.2×10^{-2} m, and thickness of 1.1×10^{-4} m. Each layer has a pin-fin enhanced micro-gap on top of it. Thickness of micro-gaps are the height of Pin-fins, which is 3×10^{-4} m, as all four layers are stacked together and connected through pin-fins.

Staggered Pin-fins with diameter of 1×10^{-4} m has longitudinal and transverse pitch of 2.2 and 1.1×10^{-4} m, as shown in Fig. 30. Deionized water as coolants is individually pumped through four micro-gaps, with 1 W pumping power each. Parameters set in the model are listed in the Table 15.

Table 15: Parameters for the model.

T_{amb}	293 K	T_{in}	298 K
h_{amb}	10 W/m^2 K	T_{ini}	298 K
L	12000×10^{-6} m	h_{hts}	550 W/m^{2}K
d_{Si}	100×10^{-6} m	W	16000×10^{-6} m
d_{SiO2}	10×10^{-6} m	H_{pins}	300×10^{-6} m
D_p	100×10^{-6} m	S_{lo}	220×10^{-6} m
Cp_{Si}	707 J/kg/K	S_{tr}	110×10^{-6} m
k_{Si}	149 W/mK	ρ_{Si}	2330 kg/m^3
Cp_{SiO2}	730 J/kg/K	k_{SiO2}	1.4 W/mK
ρ_{SiO2}	2200 kg/m^3		

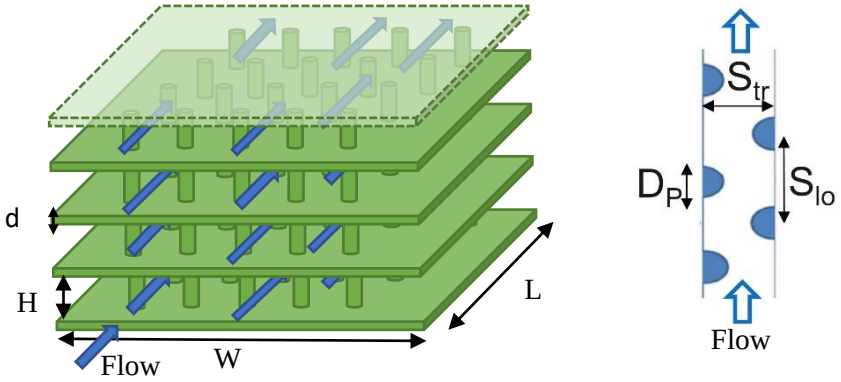


Figure 30: Configurations of 3D-SICs model with pin-fins.

5.3.2 Applied Power Maps

In this thesis, doubled the power map of Penryn [60], a 45 nm Intel Core 2 Duo processor, with 95 W for each core and 8 W for each cache have been implemented in the compact model. The total power of each layer with two cores and two caches is 206 W. Each layer contains two identical cores and two identical caches, but located in reverse arrangements. Two cores in the first and third layer are located on the one side, however, cores in the second and the fourth layer are located on the opposite side. All the power maps of the four layers are shown in Fig. 31.

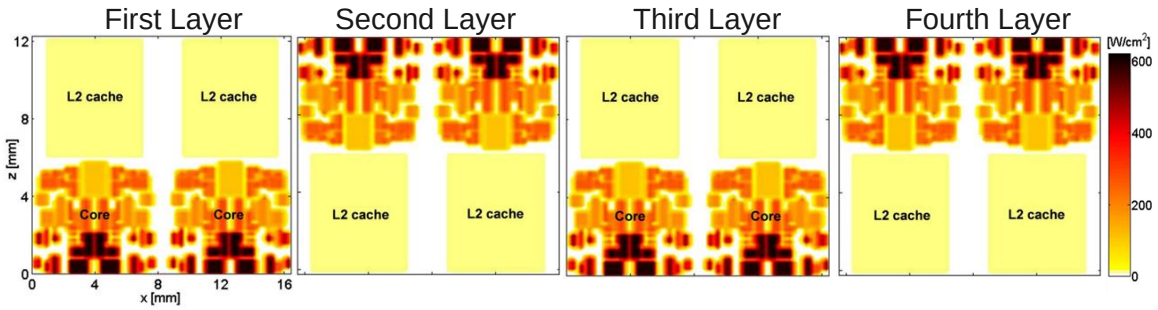


Figure 31: Power maps of four chip layers.

5.4 Performance Analysis of 3D-SIC Compact Model

In this section, both thermal and electrical leakage simulations are performed under steady state and transient state. The feature of various coolant directions in micro-gaps is introduced in the section 5.4.1 under steady state. Transient simulation feature with constant power maps is presented in the section 5.4.2. Transient simulation with temporally varying power map is introduced in the section 5.4.3.

5.4.1 Various Flow Directions of Compact Model

In addition to the accurate transient simulation feature, this compact thermal model also has a multi-flow direction feature to achieve more efficient cooling performance for layers with a non-identical power map. Cooling enhancement can be observed by comparing two cases with the same power map and pumping power, but with different flow directions. Figs. 32 (a) and (b) show the temperature field and flow directions of all layers. Because of the different flow directions in Figs. 32 (a) and (b), the temperature fields of the layers with the same power distribution are also different.

Table 16 shows the maximum temperature difference of all four layers in the two cases. In the opposite flow direction, the maximum temperature decreases 5 °C for the second layer, and 3.6 °C for the fourth layer. By contrast, in the same flow direction, the maximum temperatures of the other two layers are relatively stable. These results suggest that the flow direction between each layer affects the cooling performance based on non-uniform power maps. When the hotspots of the non-uniform power map are located in the upstream, the temperature of layers decreases. Therefore, this function can be used to achieve the best cooling effect for each layer by changing the flow direction based on

power map distribution. Table 16 also illustrates the temperature differences with and without thermal-electrical co-design in steady state. Realistic maximum chip temperatures are normally 0.5 to 1 ºC lower than the simulation results from thermal only compact thermal model, because of updated power map by implementing maximum temperatures. Table 16 also includes leakage power of each layer based on the realistic average chip temperature. Although case 2 with various flow directions has lower maximum chip temperatures, it has a higher leakage power which is considered by the average chip temperature for the leakage of entire chip.

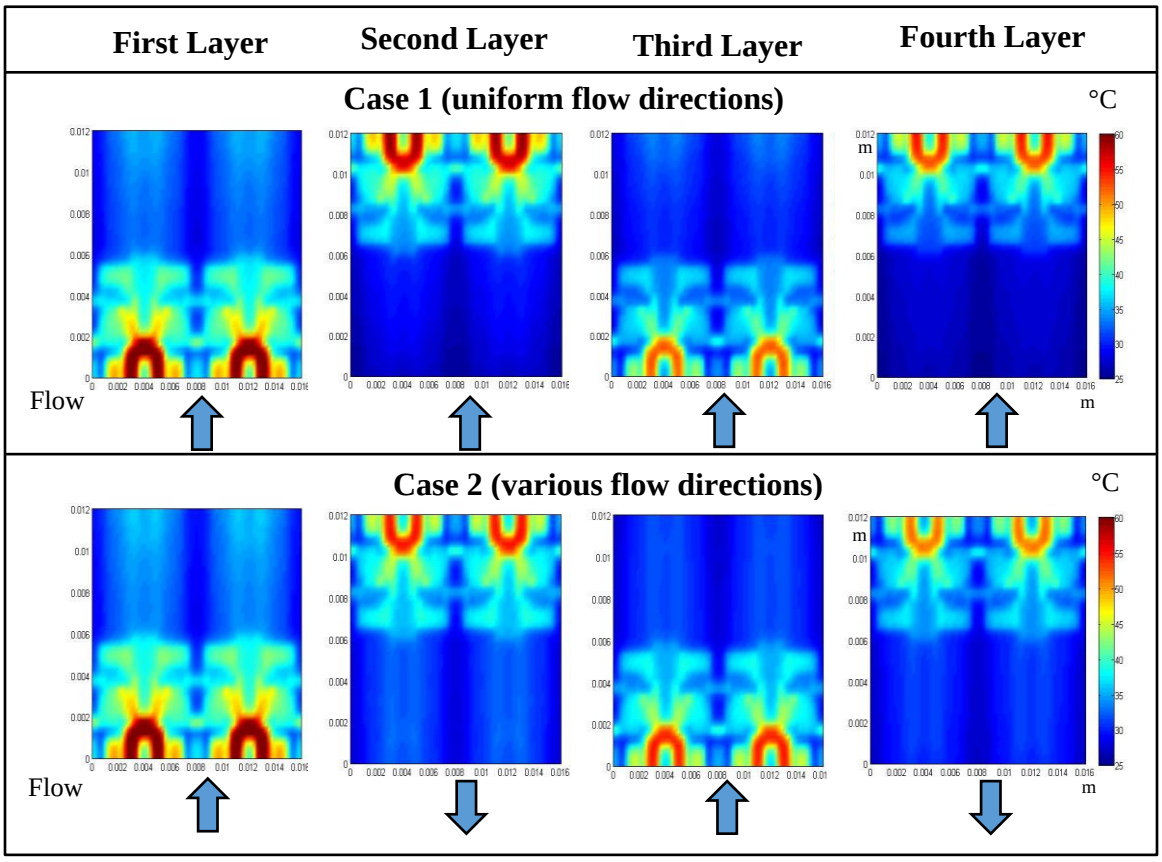


Figure 32: Temperature fields of steady state models with (a) uniform and (b) various flow directions.

Table 16: Maximum temperatures with different flow directions with and without thermal-electric co-design.

		Maximum temperature and leaking power			
		First Layer	Second Layer	Third Layer	Fourth Layer
Case 1 (Fig.32 (a)): Uniform flow directions	Thermal model only	62.3 (°C)	60.0 (°C)	52.6 (°C)	55.3 (°C)
	With thermal-electrical co-design	61.8 (°C)	59.1 (°C)	52.1 (°C)	54.4 (°C)
	Electrical Leakage	31.2 (W)	30.9 (W)	30.9 (W)	30.8 (W)
	Total Leakage	123.8 (W)			
Case 2 (Fig.32 (b)): Various flow directions	Thermal model only	62.6 (°C)	55.1 (°C)	54.8 (°C)	51.6 (°C)
	With thermal-electrical co-design	62.2 (°C)	54.6 (°C)	54.3 (°C)	51.2 (°C)
	Electrical Leakage	31.3 (W)	31.0 (W)	31.0 (W)	30.9 (W)
	Total Leakage	124.2 (W)			

5.4.2 Transient Feature of Compact Model

One of the features of the compact model is that it can simulate the transient temperature field. An important parameter setting for evaluating the thermal performance of the transient model is the power map, or the spatial heat flux distribution. The parameters required in the compact model appear in Table 15. Fig. 33 shows the transient temperature field with and without electrical co-design of all four layers at time 20, 40, and 80 seconds. At t= 20 seconds, the temperatures of a majority of the area of the chip are below 40 °C, but only parts of the two cores have reached or close to 50 °C. After 20 seconds, because of heat conduction within each layer, the maximum temperatures of each layer increase, and the areas of temperatures higher than 50 °C also increase. Besides the heat conduction within each layer, heat conduction through pin fins between the layers in the vertical direction also has significant thermal effects. As indicated at 80 seconds, non-uniform temperatures of the two caches with uniform power maps occur because of the vertical heat conduction through the cylindrical pin fins. All the realistic maximum chip temperatures with electric co-design in the 3D-SICs at each time step are normally 0.5 to 1.5 ºC lower than the simulation results from thermal only compact thermal model, because of updated power map by implementing maximum temperature of each layer into electrical co-design function. Leakage power of each layer based on the realistic average chip temperature has been presented for each time step.

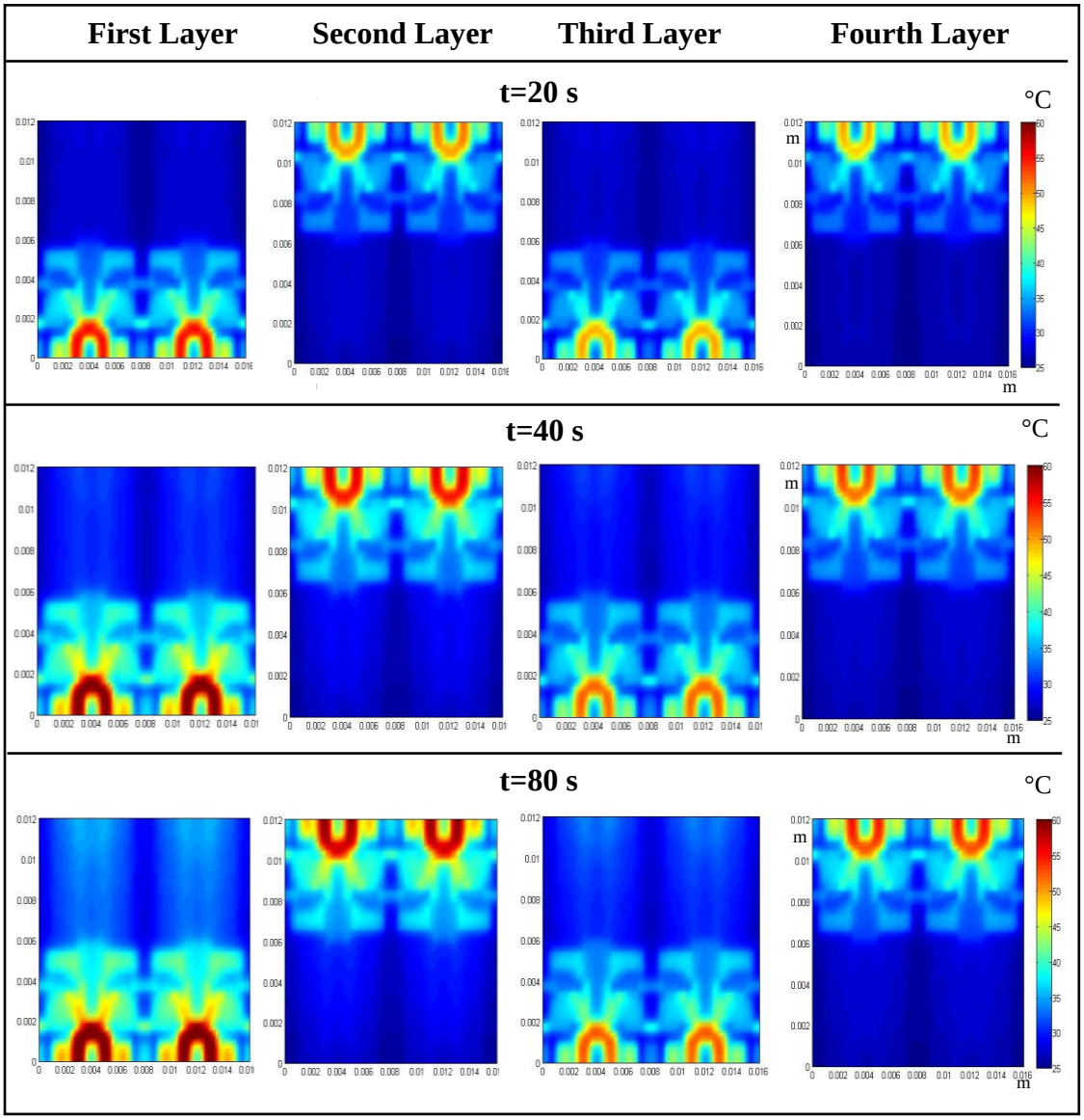


Figure 33: The temperature field of the transient model with fluidic cooling.

Table 17: Maximum temperatures and leaking power of transient model with and without thermal-electric co-design.

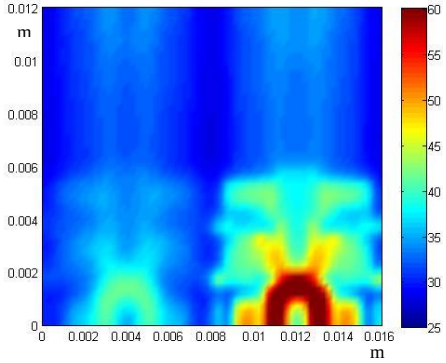
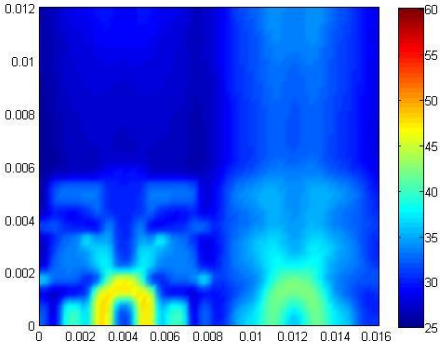
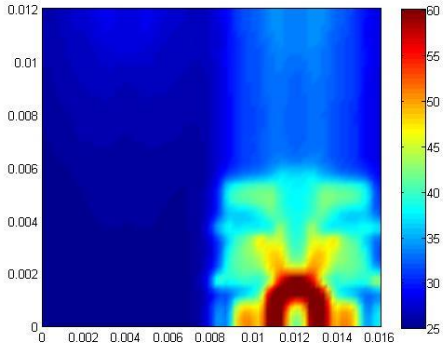
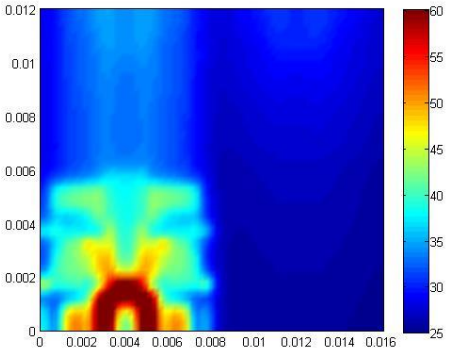
		Maximum temperature and leaking power			
		First Layer	Second Layer	Third Layer	Fourth Layer
t= 20 s	Thermal model only	55.5 (°C)	51.4 (°C)	49.7 (°C)	49.8 (°C)
	With thermal-electrical co-design	53.7 (°C)	49.7 (°C)	48.3 (°C)	48.1 (°C)
	Electrical Leakage	30.7 (W)	30.6 (W)	30.6 (W)	30.6 (W)
t= 40 s	Thermal model only	60.9 (°C)	56.7 (°C)	52.2 (°C)	53.7 (°C)
	With thermal-electrical co-design	59.8 (°C)	55.4 (°C)	51.5 (°C)	52.5 (°C)
	Electrical Leakage	31.0 (W)	30.8 (W)	30.8 (W)	30.7 (W)
t= 80 s	Thermal model only	62.2 (°C)	59.6 (°C)	52.6 (°C)	55.1 (°C)
	With thermal-electrical co-design	61.7 (°C)	58.6 (°C)	52.1 (°C)	54.2 (°C)
	Electrical Leakage	31.1 (W)	30.9 (W)	30.8 (W)	30.7 (W)

5.4.3 Various Heating Periods Feature of Compact Model

In addition to variable flow direction, the transient power map function has been built in the compact model. The mower map distribution of each layer can differ, which was mentioned before, and change with time. Employing the transient power map, the compact model can simulate the temperature fields of real-time power maps. In this paper, the four-layer power map, including two cores and two caches for each layer, will change so that it can simulate real-time workloads. In addition to the power map parameters, the pumping powers for fluidic cooling between all layers remain constant and at 1 W.

Table 18 shows the temperature fields of the first layer, that is, the simulation results in two heating periods. Initially, both cores in this layer are working at full capacity. Then the left core turns off as the beginning of the first period. After 60 seconds, the active cores are switched at the beginning of the second period. Hence, period 1 is 0 to 60 seconds and period 2 is 60 to 120 seconds, and then the temperature field achieves steady state. As only one core and one cache are active in both periods, the total power for each layer is always 103 W. As the active core changes from one period to the next, Table 15 shows the temperature transition at the beginning of the second period. Users can determine the resolution of the transition based on their requirements.

Table 18: Parameters and results for the heating periods.

First Layer	Heating Power Period 1	Heating Power Period 2
Temperature Field (°C)	 At t=0 second	 At t=70 second
	 At t=60 second	 At t=120 second

5.5 Summary

In chapter five, a compact co-design model for pin-fin enhanced micro-gap liquid cooling has been built. This steady and transient state model considers both thermal and electrical perspectives.

From the thermal perspective, in contrast to other compact models for pin-fin enhanced micro-gap model considering the pin-fin structures as porous media, our model considers heat conduction between layers through pins and heat convection from pin

surfaces, based on pin-fin configurations, which contribute to accurate and reliable temperature results within the tested pin-fin configuration ranges. 3D-SIC configurations can be set in the model including: layer numbers, layer dimensions, layer materials, pin configurations, pin materials and specially varying power map for each layer. Liquid coolant configurations can be set in the model including: coolant properties, pumping power and flow direction for each micro-gap. The model can rapidly simulate the steady state within 2 minutes, and transient state within 15 minutes, even if the power map may be varied with time.

From the electrical co-design perspective, the compact model can simulate the actual leakage power by deducting the over-estimated leakage power based on temperatures provided from thermal model. Then the actual chip temperatures will be updated based on the feedback of the actual chip power. Unlike temperatures generated from other compact models and CFD/HT full-scale simulation software, temperatures from this thermal-electrical co-design model are closer to chip temperatures in reality.

CHAPTER 6. MICRO-GAPS THERMOSYPHON COOLING FOR 3D-SICS

In contrast to active liquid cooling approach for both 2.5D and 3D-SICs, an experimental implementation of two-phase passive liquid cooling, miniature-thermosyphon, for 3D-SICs is presented in this chapter. Although extensive studies have studied the characteristics of miniature-thermosyphon thermal management via both simulations and experiments, none of them have implemented miniature-thermosyphon into 3D-SIC cooling. The cooling capacity of 3D-SIC thermosyphon for each layer of 3D-SICs remains unknown. In my study, multi-layered heaters with micro-gaps are served as an evaporator, a core component of the miniature-thermosyphon system. Cooling performance of this passive pumpless thermal management method has been evaluated experimentally with various characteristics of loop component, including evaporator tilting angle, rising height between condenser and evaporator, and inlet chilled water temperature of condenser in the auxiliary loop.

6.1 Two-Phase Thermosyphon For Passive Liquid Cooling

Thermosyphon is a pumpless passive cooling method based on natural convection, which circulates the coolant, and transfers heat from heat sources to a heat sink. Without pump driven coolant circulation, a thermosyphon working fluid circulates only when the driving force is larger than the friction in the loop. Pressure differences associated with the driving force and friction force are:

$$\Delta P_{driving} = gH(\rho_{downcomer} - \rho_{riser}) \tag{13}$$

$$\Delta P_{friction} = f(\dot{m}, \frac{\rho_l}{\rho_v}, D_i, H, \dots) \tag{14}$$

6.2 Miniature-Thermosyphon for 3D-SICs

As mentioned in Chapter 1, 3D-SICs have multi-chip stacked structures, each generating high heat fluxes in limited space. Because of these characteristics, most of the thermal management solutions for 3D-SICs, focus on forced convection. Passive liquid cooling using dielectric working fluids in these applications offers several advantages. Fluid leak will not damage electronics;

--Direct contact chip level liquid cooling possible, which eliminates several thermal contact resistances;

--Passive cooling eliminates pump failure concerns and provides energy savings;

--Lower maintenance due to reduced system complexity;

--Less corrosion concerns.

In implementing a miniature-thermosyphon for 3D-SICs, the heat sources from stacked chips with micro-gaps, serve as an evaporator, the core self-driven component for miniature-thermosyphon loop. As no known previous studies focus on implementing thermosyphon on 3D-SICs, the cooling capacities for each layer of 3D-SICs remain unknown and will be investigated in this chapter.

6.3 Experimental Setup

In this section, an experimentally investigated miniature-thermosyphon system, including a main loop filled with dielectric coolant and an auxiliary loop filled with DI water, has been introduced. A 3D-SIC evaporator as the core component of the miniature-thermosyphon system has been illustrated in 6.3.2.

6.3.1 Loop design and its future application

Fig. 34 (a) shows the schematic diagram of a miniature-thermosyphon loop that is experimentally investigated. It consists of one main loop filled with Notec 7200 coolant (3M), and one auxiliary loop filled with DI water. In the main loop, there are mainly two components: 3D-SICs, the heat sources, serves as an evaporator to generate self-driven coolant flow for 3D-SICs thermal dissipation via natural convection, and a liquid-to-liquid heat exchanger to condense the coolant vapor. The evaporator is placed below the condenser. The height difference between the condenser (Chemglass) and evaporator is maintained at 28 cm and 56 cm. Novec 7200 coolant vaporizes in the evaporator by absorbing heat from heaters in the 3D-SCIs. Under natural convection, it rises up to the condenser. In the glass liquid-to-liquid condenser, the dielectric vapor condenses to saturated liquid, and then returns to the evaporator under gravity.

T-type thermocouples (Omega) with a diameter of 3.175 mm are placed on foil heaters simulating 3D-SICs to measure chip temperatures and are placed in the main loop to measure Novec 7200 dielectric coolant temperatures at the inlets and outlets of both evaporator and condenser. This condenser, liquid to liquid heat exchanger, connects both the Novec 7200 dielectric coolant main loop and DI water side loop, which includes a water

bath and a flow meter. A water bath with pump (LAUDA, RM6) provides DI water with constant flow rate of 4.7 g/s at set temperatures of 10 °C, 15 °C, and 20 °C. A flow meter (KING S/N: 737701000014), calibrated for DI water at room temperature, provides the auxiliary loop flow rate measurement. DI water auxiliary loop receives the heat transferred from condensed Novec 7200 vapor in the main loop. Insulation is applied to the main loop to decrease heat loss to the ambient. Both Fig. 34 (a) and (b) share the same altitude indicator on the right of this figure, and Fig. 34 (b) is an illustration of potential application of this 3D-SIC thermosyphon thermal management. 3D-SIC is the evaporator in our tested loop, as indicated in Fig. 34 (a). This stacked characteristic could be applied in the 1U-rack because of their small thickness. All 1U-racks at each layer can adopt this miniature-thermosyphon passive liquid cooling method and the vaporized dielectric vapor will rise to the condenser which is placed on top the server. Data center building chilled water lines connect the other side of the liquid to liquid condenser to reject the heat generated by 3D-SICs to ambient.

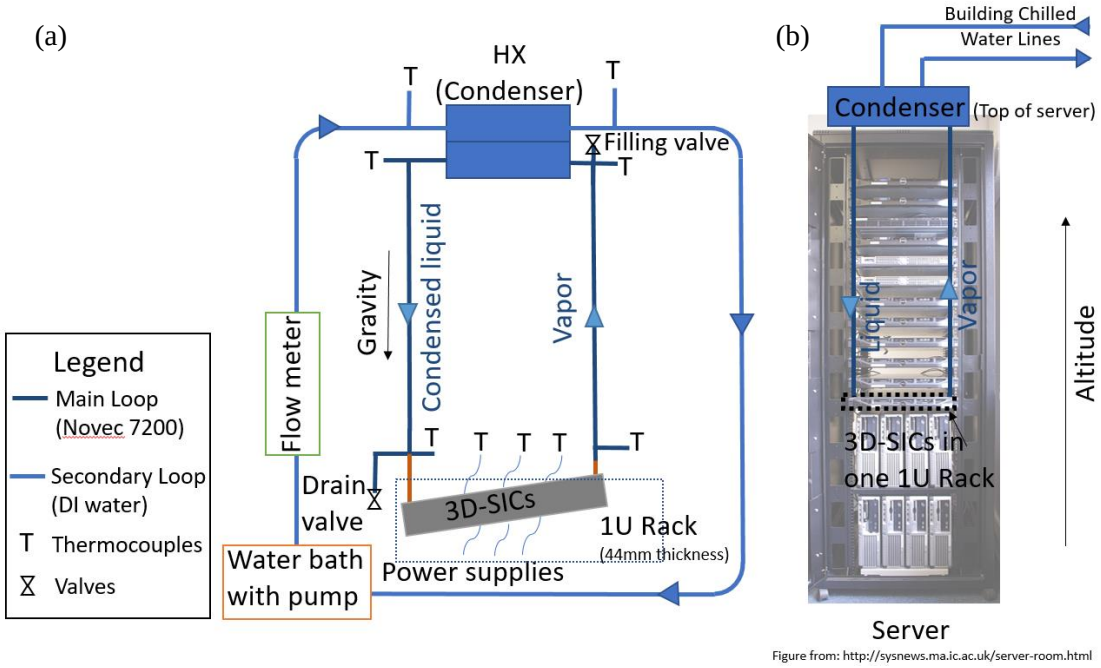


Figure 34：(a) Schematic diagram of thermosyphon loops (b) Potential application of 3D-SIC miniature-thermosyphon thermal management in data center.

6.3.2 3D-SIC Evaporators

3D-SIC evaporators, assembled in our lab, have three heating layers with two T-type thermocouples on each layer. Each layer includes a 25.4 x 25.4 mm, polyimide thin film heater (All Flex Co.), which is attached to a 25.4 x 76.2 mm high-yield copper sheet (REVERE certified 99.94% Cu,) with thickness of 0.406 mm. Two micro-gaps with thickness of 0.178 mm are between these three layers. These layers with micro-gaps have tilt angles of 30º and 60º for each evaporator. This evaporator is connected to the Novec 7200 dielectric main loop via copper tubes with inside diameter of 11.1 mm. Dielectric coolant fills the evaporator in the main loop, and flow direction is from the lower side to the higher side because of reduced density due to heating.

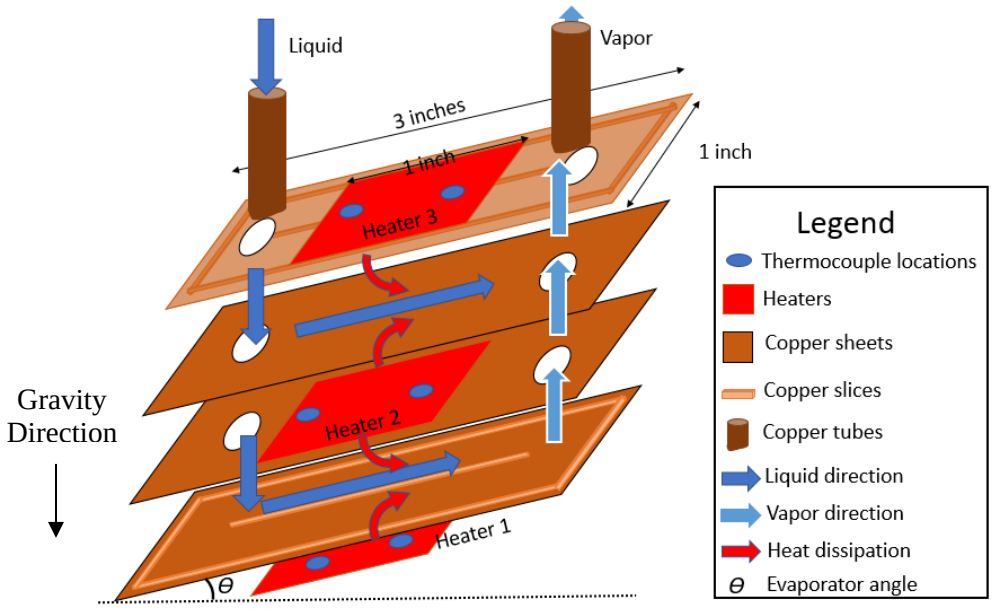


Figure 35: Schematic diagram of 3D-SICs evaporator in the miniature-thermosyphon loop.

6.4 Miniature-Thermosyphon Performance

Fig.36 indicates four characterises that have been investigated in this thesis. To begin with, cooling capacity always play an important role in the evaluation of any thermal management method. Two power maps have been implemented in our evaporators. The total power of the first power map is 48.7 W with 18.2 W, 19.5 W and 11 W for top middle and bottom heaters respectively. The Second power map with total power of 54.3 W that is about 10% higher than the first power map. In addition to the power input investigation, tilting angle of evaporator is another factor considered, because it could contribute to difference of vapor rising speed and further affect thermosyphon cooling capacity. Inclinations of 0°, 30° and 60° have been investigated. In the main loop, altitude difference between evaporator and condenser with different potential energy of condensed coolant is an important factor for the function of thermosyphon loop. A larger altitude difference

would contribute to higher flow rate of coolant in the main loop, as it has more potential emery to overcome the tube friction resistances.

Fig. 37 shows the experimental set up with both main and auxiliary loops. Fig. 37 (a) has the height difference as 56 cm, with data acquisition systems (Keysight 34970A) and power supplies (Agilent E3649A and RSR M10-SP-503E) on the left side and water bath (Lauda RM6) on the right side. Fig. 37 (b) has the height difference of 28 cm and the main loop including condenser have been covered by thermal fiberglass insulation material (fiberglass, k=0.045 W/mK at 350K). The last factor investigated is the condenser inlet DI water temperature in the auxiliary loop. This chilled water temperature can be controlled by water bath at 10, 15 and 20 ^{o}C to simulate data center applications.

To ensure repeatability temperature measurements, all performance evaluations have been repeated. Temperature differences between these repeated tests are generally within $\pm$0.5 ^{o}C, with the maximum difference of 1.1 ^{o}C. All the thermocouples are calibrated in a mixture of ice and water, and water bath at 20 ^{o}C, 40 ^{o}C, 60 ^{o}C and 80^{o}C.

As thick thermal insulation layers (25 mm) have been incorporated, the majority (condenser inlet DI water at 10 ^{o}C: 85-95%; condenser inlet DI water at 20 ^{o}C: 75-85%) of the power provided to the evaporator is removed by the DI water filled auxiliary loop through the condenser.

① 3D-SICs (evaporator) power densities:

	Top	Middle	Bottom	Total
Power 1(W)	18.2	19.5	11	48.7
Power 2(W)	20.1	21.6	12.5	54.3

② 3D-SICs (evaporator) tilting angles:
60° and 30°.

③ Riser height above 3D-SICs (evaporator):
28 cm and 56 cm.

④ Condenser inlet chilled water temperatures:
10 °C, 15 °C, and 20 °C.

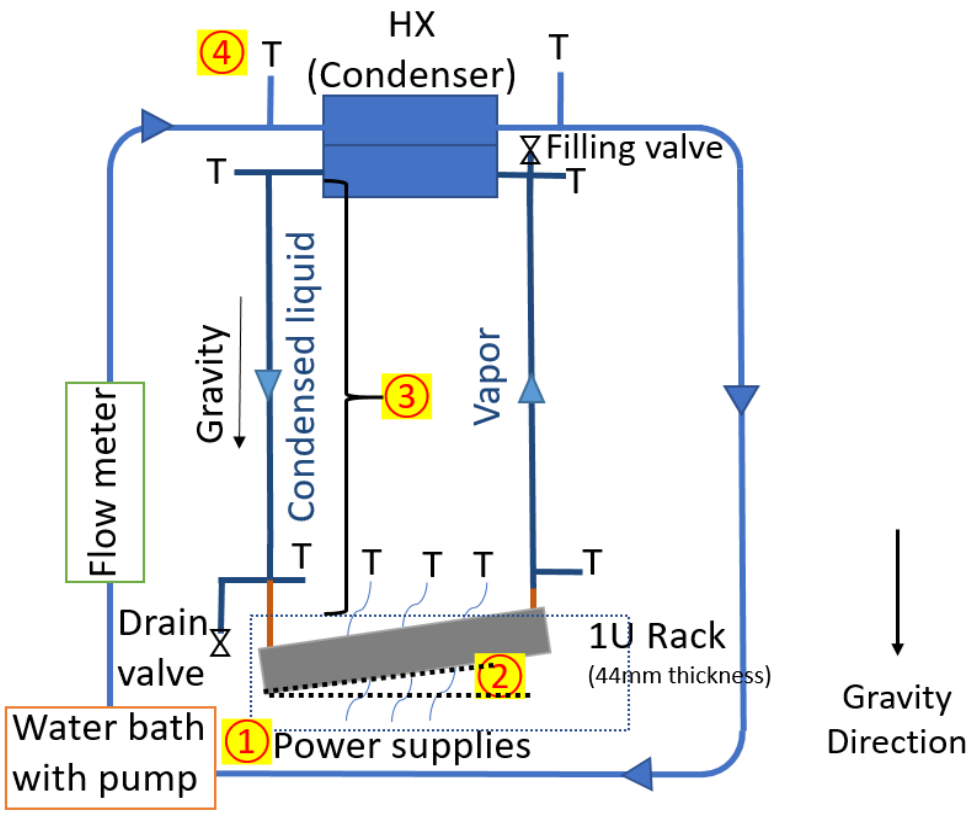


Figure 36: Investigated characteristics of 3D-SICs miniature-thermosyphon liquid cooling.

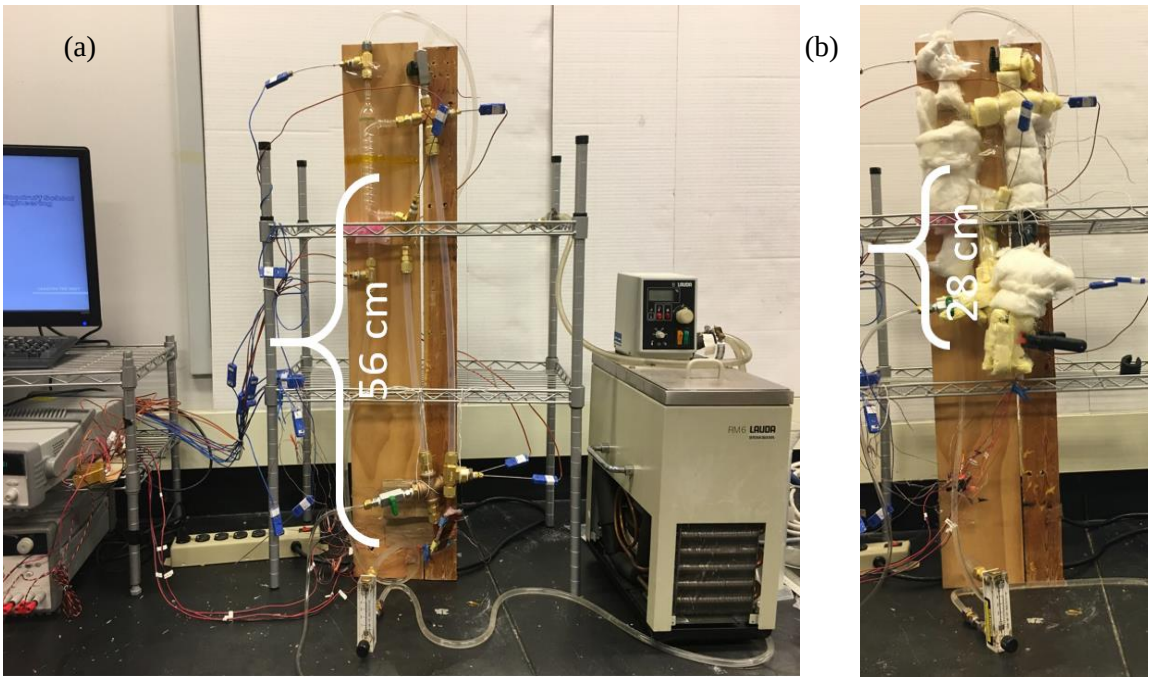


Figure 37: Two heights of miniature-thermosyphon testing loops: (a) 56 cm; (b) 28 cm.

6.5 Results and Discussion

The cooling performance of this 3D-SIC miniature-thermosyphon loops has been evaluated experimentally with various loop characteristics in this section. These evaluated characteristics include evaporator and condenser inlet temperatures, height differences between condenser and evaporator, 3D-SIC heat flux, and its tilting angles. Bubble visualizations at the outlet of 3D-SICs are included as well.

6.5.1 Evaporator Inlet Temperatures of Novec 7200 Coolant

Fig. 38 illustrates the effects of power map, height differences, and condenser inlet temperatures on the evaporator inlet temperatures, for condenser inlet temperatures of 10 ºC, 15 ºC and 20 ºC. The evaporator inlet temperatures of the Novec 7200 dielectric coolant are presented. For a given condenser inlet temperature, evaporator inlet

temperatures are indicated by four bars with various working conditions: both green and blue bars have the same height difference at 56 cm, but with different power as 49 W and 54W respectively; yellow and orange bars have the same height difference at 28 cm, but with different power as 49 W and 54W respectively. At a given condenser inlet temperature, evaporator inlet temperatures of Novec 7200 dielectric coolant are slightly higher with higher power of 54 W. However, with the same power map, height difference does not affect evaporator inlet temperatures. Evaporator inlet temperatures of all four conditions increase with increasing condenser inlet temperatures.

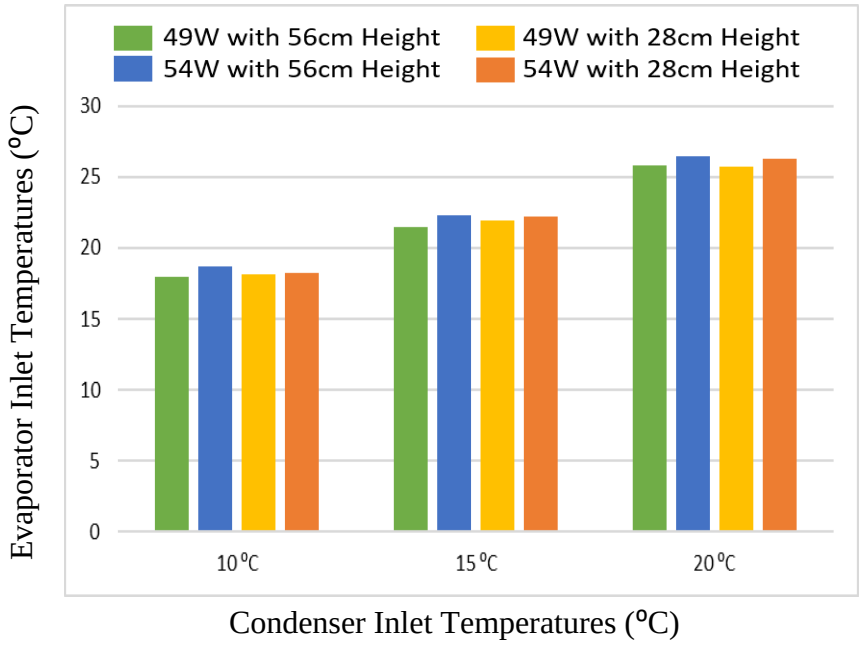


Figure 38: Effects of condenser inlet temperatures on evaporator inlet temperatures.

6.5.2 Evaporator Outlet Temperatures of Novec 7200 Coolant

Fig. 39 illustrates the effects of power map, height differences, and condenser inlet temperatures on the evaporator outlet temperatures for condenser inlet temperatures of 10 ºC, 15 ºC and 20 ºC. The evaporator outlet temperatures of the dielectric coolant are presented. For a given condenser inlet temperature, evaporator inlet temperatures are indicated by four bars with various working conditions: both green and blue bars have the same height difference at 56 cm, but with different power as 49 W and 54W respectively; yellow and orange bars have the same height difference at 28 cm, but with different power as 49 W and 54 W respectively.

At a given condenser inlet temperature, height differences have significant effects on evaporator outlet temperatures. Both cases with 28 cm height difference have 76 ºC evaporator outlet temperatures, which is the atmosphere saturation temperature. However, both cases with 56 cm height difference have 64-66 ºC evaporator outlet temperatures. Higher power would contribute to higher evaporator outlet temperatures. However, for the 28 cm height, increase in power does not affect evaporator outlet temperatures, as saturation conditions are achieved at the outlet of the evaporator. Evaporator outlet temperatures for both powers with 56 cm height difference increase with increasing condenser inlet temperatures. However, the two cases with 28 cm height difference are not affected, which means condenser inlet temperatures impact evaporator inlet temperatures only if the evaporator outlet temperatures have not reached the saturation temperature.

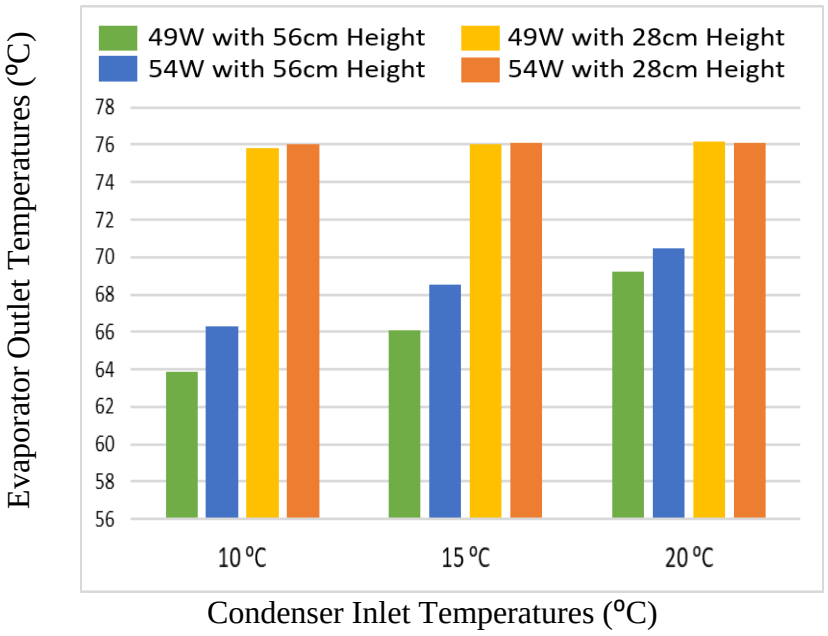


Figure 39: Effects of condenser inlet temperatures on evaporator outlet temperatures.

6.5.3 Two-phase Boiling Regimes at Evaporator Outlet

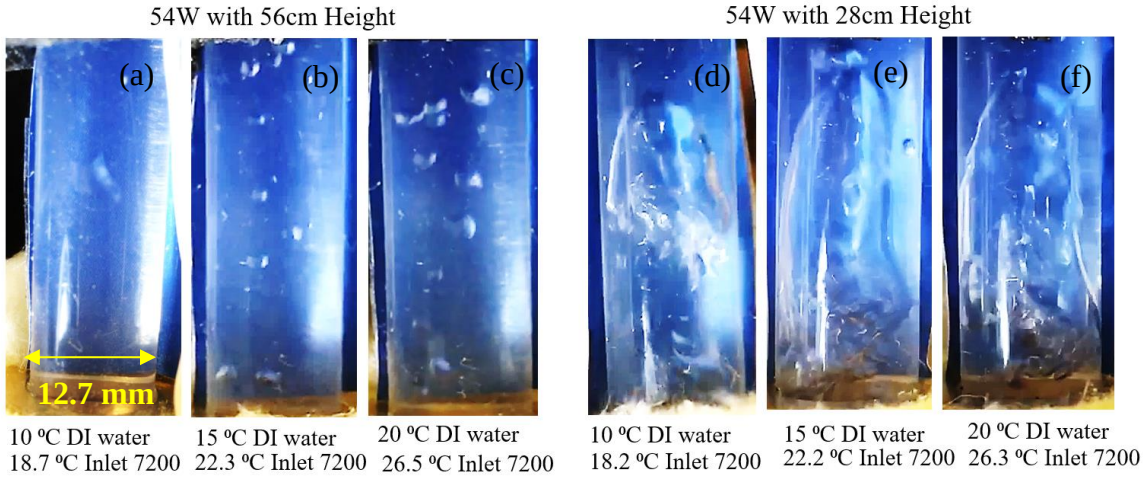


Figure 40: Bubbles at the evaporator outlet at 54 W: Height difference of 56 cm, and (a) condenser inlet temperature at 10 °C; (b) condenser inlet temperature at 15 °C; (c) condenser inlet temperature at 10 °C; Height difference of 28 cm, and (d) condenser inlet temperature at 10 °C; (e) condenser inlet temperature at 15 °C; (f) condenser inlet temperature at 10 °C.

Fig. 40 presents visualizations of two phase flow at the outlet of evaporator. Coolant temperatures for this condition have been illustrated in Fig. 39. For Fig. 40 (a), (b), and (c) these are 66 °C, 68 °C and 70 °C respectively. In Fig. 40 (a), intermittent bubbles can be seen every 2 seconds. More vapor bubbles can be seen with the increase of condenser inlet temperature from 10 to 20 °C. Higher evaporator inlet and outlet coolant temperatures could also contribute to the increasing vapor quality. The flow regime is bubbly flow, and heat transfer is via subcooled boiling. Similarly, as can be seen from Fig. 38, coolant exit temperature in Figs. 40 (d), (e), and (f) keep at 76 °C saturation temperature.

In contrast with the Fig. 40 (a), (b), (c) with a height difference of 56 cm, larger vapor bubbles can be observed in Fig. 40 (d), (e), and (f) with height difference of 28 cm. In Fig. 40 (d), a vapor slug occupies more than 30% of the volume of this tubing section. Larger vapor bubbles (higher vapor quality) can be seen with increase in condenser inlet temperature from 10 to 20 °C, and large vapor bubbles almost fill the entire volume of this tubing section in Fig. 40 (e) and (f). Higher coolant evaporator inlet and outlet temperatures could also contribute to the increasing vapor bubbles, especially when the temperature at the evaporator outlet reaches saturation conditions. Flow patterns in Fig. 40 (d), (e), and (f) are characterized as slug flow under saturated nucleate boiling.

6.5.4 Height Difference Effects on Heater Temperatures

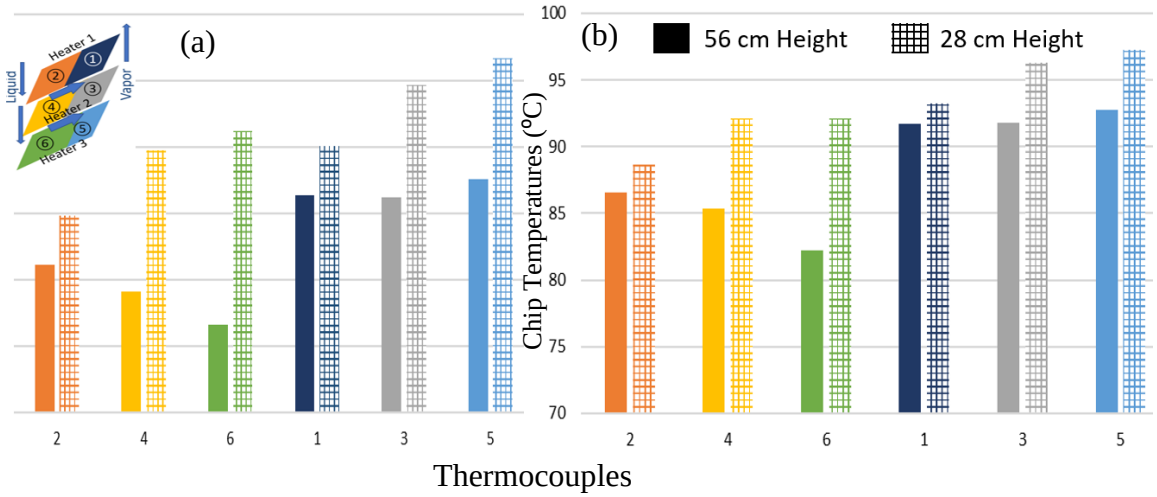


Figure 41: Height difference effects on heater temperatures with 54 W total power: (a) condenser inlet temperature at 10 °C; (b) condenser inlet temperature at 20 °C.

As mentioned in Section 6.3.2, heater 1 is the top heater cooled by one liquid filled micro-gap under it, heater 2 is located in between two liquid filled micro-gaps, and heater 3 as the bottom heater is cooled by one liquid filled micro-gap above it. Thermal insulation layers have been incorporated on top of heater 1, and at the bottom of heater 3. As this 3D-SIC simulated structure has three heaters with 6 thermocouples in our evaporator, six chip temperatures can be measured. Sequence and indicating colors of these six thermocouples are listed in Table 16.

Fig. 41 illustrates height difference effects at the six heater locations, with 54 W total power. Solid filled bars represent the 56 cm height difference, and grid filled bars the 28 cm height difference. In Fig. 41 (a) with condenser inlet temperature at 10 °C and 56 cm height difference, thermocouples 2, 4, and 6 decrease from top heater to bottom heater, and these temperatures are lower than others. Thermocouples 1, 3 and 5 have similar

temperatures, and are relatively higher than others. In Fig. 41 (a) with condenser inlet temperature at 10 ºC and 28 cm height difference, similarly, thermocouples 2, 4, and 6 are lower than others, but increase in value from top to bottom heaters. Thermocouples 1, 3 and 5 show higher temperatures, which increase from top to bottom heaters. The temperature of thermocouple 6 is even higher than the temperature of thermocouple 1. Height difference could dramatically affect the temperature trend of chips in 3D-SICs layers. Similarly, Fig. 41 (b) with higher condenser inlet temperature at 20 ºC, shows similar data trends as in Fig. 41 (a), but with higher temperature of all thermocouples. Lowest temperature is at thermocouple 6 with 56 cm height difference, increasing from 77 ºC to 82 ºC with the increasing of condenser inlet temperature from 10 ºC to 20 ºC. Two thermocouples achieve the highest temperature around 97 ºC in Fig. 41 (b) with 28 cm height difference.

Table 19: Sequence and indicating colors of six thermocouples.

		Upstream of Coolant	Downstream of Coolant
Heater 1	Numbered as	2	1
(Top Heater)	Indicated as	Orange	Dark Blue
Heater 2	Numbered as	4	3
(Middle Heater)	Indicated as	Yellow	Grey
Heater 3	Numbered as	6	5
(Bottom Heater)	Indicated as	Green	Light Blue

6.5.5 *Condenser Inlet Temperature Effects on Chip Temperatures*

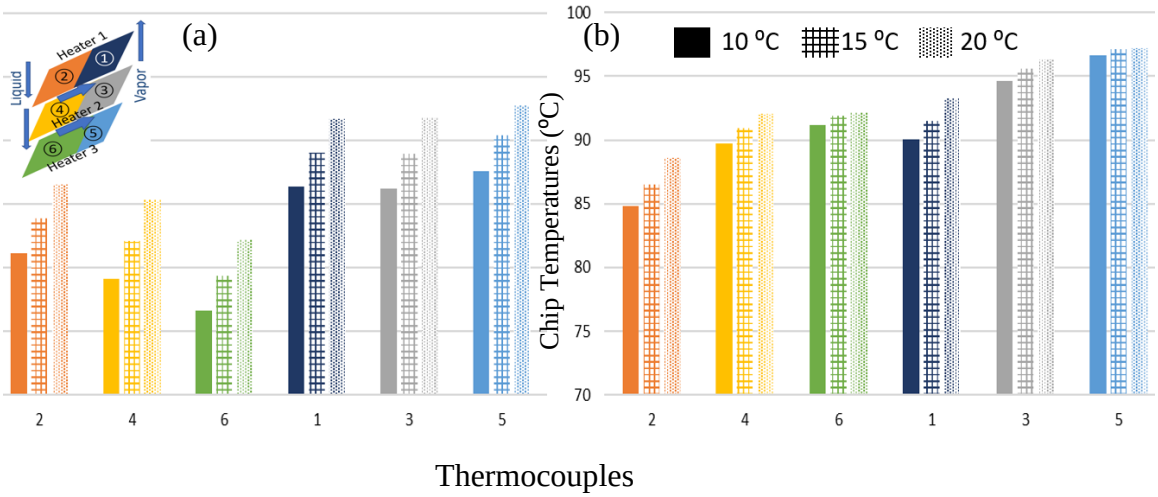


Figure 42: Condenser inlet temperature effects on chip temperatures with 54 W total power for two height differences: (a) 56 cm; (b) 28 cm.

Fig. 42 illustrates condenser inlet temperature effects on chip temperatures with 54 W total power. In Fig. 42 (a) with 56 cm height difference, upstream thermocouples 2, 4, and 6 decrease from top heater to bottom heater, and these temperatures are lower than others. Thermocouples 1, 3 and 5 have similar temperatures and are relatively higher than others. All the temperatures increase with increasing condenser inlet temperatures. Fig. 42 (b) with lower riser height of 28 cm shows opposite temperature trends. Upstream thermocouples 2, 4, and 6 increase from top heater to bottom heater, and these temperatures are lower than others, except thermocouple 6, which is even higher than thermocouple 1. Downstream thermocouples 1, 3 and 5 increase from top heater to bottom heater as well, and are relatively higher than others. Similarly, all temperatures increase with higher condenser inlet temperatures.

6.5.6 Power Effects on Chip Temperatures

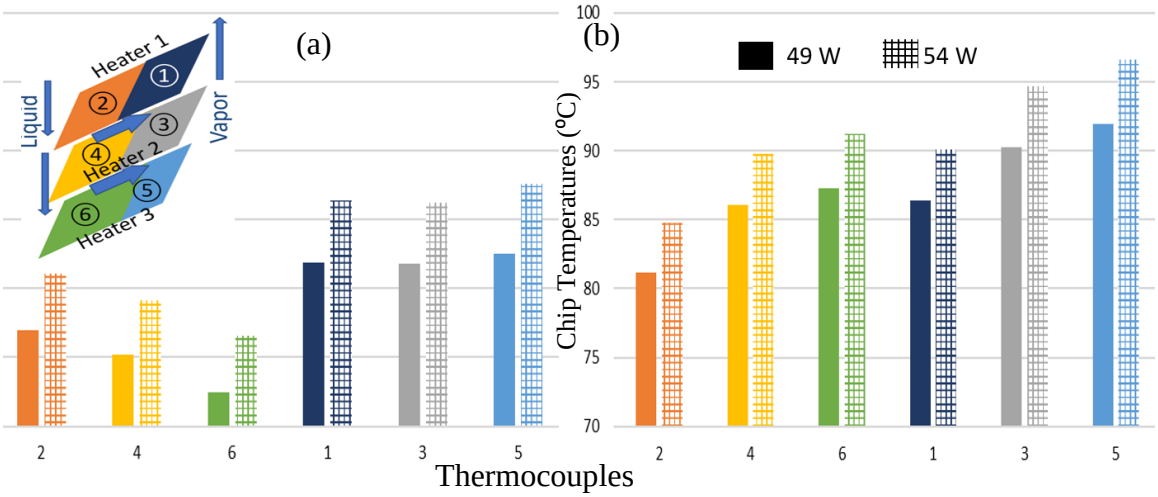


Figure 43: Power effects on chip temperatures for height differences of: (a) 56 cm; (b) 28 cm.

Fig. 43 illustrates evaporator power effects on chip temperatures for two height differences. In Fig. 43 (a) with 56 cm height difference, upstream thermocouples 2, 4, and 6 decrease from top heater to bottom heater, and these temperatures are lower than others. Thermocouples 1, 3 and 5 have similar values, and they are relatively higher than others. All the temperatures with higher power input. In contrast to Fig. 43 (a), in Fig. 43 (b) with a lower height difference of 28 cm, opposite temperature trends are seen. Upstream thermocouples 2, 4, and 6 increase from top heater to bottom heater. These temperatures are lower than others, except thermocouple 6, which is even higher than thermocouple 1. Downstream thermocouples 1, 3 and 5 increase from top heater to bottom heater, and are relatively higher than others. Similarly, compared to Fig. 43 (a) with height difference of 56 cm, all the temperatures in Fig. 43 (b) with a height difference of 28 cm increase with input power, but show weaker sensitivity.

6.5.7 Tilting Angle Effects on Chip Temperatures

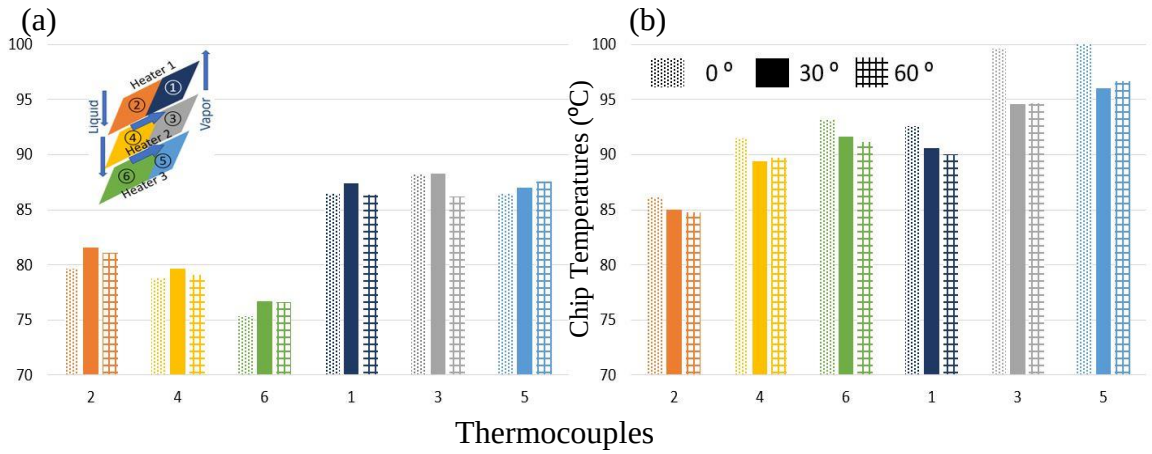


Figure 44: Tilting angle effects on chip temperatures with condenser inlet temperature at 10 °C: (a) Height difference of 56 cm;(b) Height difference of 28 cm.

Fig. 44 illustrates tilting angle effects on chip temperatures with two height differences. In Fig. 44 (a) with 56 cm height difference, temperatures of upstream thermocouples 2, 4, and 6 decrease from top heater to bottom heater, and these temperatures are lower than others. Thermocouples 1, 3 and 5 have similar temperatures and are relatively higher than others. At each heater location, temperatures of various tilting angles are similar and within 2 °C temperature difference. Evaporator with the tilting angle at 0° has lower temperature at all the upstream location, such as temperatures of thermocouples 2, 4 and 6, and thermocouple 1 and 5 at the downstream.

In contrast to the lower chip temperatures of evaporator with tilting angle at 0° in Fig. 44 (a), Fig. 44 (b) with a lower height difference of 28 cm shows opposite cooling performance. For each evaporator tilting angle design, temperatures of upstream thermocouples 2, 4, and 6 increase from top heater to bottom heater and these temperatures

are lower than others, except thermocouple 6, which is even higher than thermocouple 1. Temperatures of downstream thermocouples 1, 3 and 5 increase from top to bottom heaters, and are relatively higher than others. In contrast to better cooling performance of evaporator with tilting angle at 0º at height of 56 cm in Fig. 44 (a), the evaporator with tilting angle at 0º have higher temperatures of all the heater location. Temperatures of this evaporator design at the downstream location, such as heater 3 and 5 achieve 100 ºC because of the lower flow rate at the lower rising height and higher (saturated) outlet evaporator temperature.

6.6 Summary

Miniature-thermosyphon passive liquid cooling was implemented for 3D-SICs as presented in chapter six. A three-layer 3D-SIC with two 178 μm thickness micro-gaps serves as evaporator in a closed thermosyphon loop.

Unlike other thermosyphon studies with only one power supplied to evaporator and testing the their thermosyphon loop performance, three individual heaters are located in the evaporator, and six thermocouples measure both upstream and downstream parts of these heaters, as temperatures of each layer are important to 3D-SIC thermosyphon cooling performance evaluation.

The height difference between the evaporator and condenser is critical for thermosyphon cooling performance. The larger the height difference, the better the cooling performance. Upstream location would have enhanced cooling performance, and bottom layer suffers from limited cooling capacity. The temperatures of heaters on the upstream are decreasing from top layer to the bottom layer under higher height difference. On the

contrary, these temperatures are increasing from top layer to the bottom layer under shorter height difference. The temperatures of heaters on the downstream are always increasing from top layer to the bottom layer.

Condenser inlet temperatures have effects on chip temperature as well as vapor qualities after the evaporator. This finding can be useful for further server level thermal management in data centers. Not as expected, tilting angles of evaporators do not have significant effects on their temperatures, especially for the higher rising height, but the tilting angle at 0º could have limited cooling enhancement at the higher rising difference, but significant lower cooling capacity at the lower rising difference.

It is worth to mention that to achieve comparable temperatures of all three layers, the power provided for the bottom layer is about 60% of others, which implies the non-uniform cooling capacity of various layers of 3D-SICs thermosyphon thermal management.

CHAPTER 7. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

In this last chapter, conclusions, including both active and passive microfluidic thermal management methods for both 2.5D and 3D-SIC systems, are presented in the first section. Localized single phase liquid cooling enhancement has been studied experimentally by testing four heterogeneous pin-fin structures in micro-gaps. This includes cylindrical pins and hydrofoil fins with one design of increased pin-fin density only around the hotspot area, and another design of increased pin-fin density along spanwise direction (Chapter 2). Heterogeneous pin-fin cooling enhancement has been further investigated by designing and implementing these structures in a cooling manifold for 2.5D-SIC avionic cooling application. Using dielectric working fluid of PAO, numerical parametric studies have focused on the characteristic of this manifold for heterogeneous dies in 2.5D-SICs (Chapter 3). In addition to this cooling manifold with localized cooling enhancement structures, DoE method in conjunction with CFD/HT has been implemented for systematic thermal management optimization of heterogeneous pin-fin structures in a cold plate for 2.5D-SIC multi-component system (Chapter 4). In addition to the liquid cooling thermal management method for 2.5D-SICs, both active and passive liquid cooling approaches have been studied for heterogeneous integration. A rapid execution compact thermal-electrical co-design model for multi-layer 3D-SICs has been developed. Along with realistic leakage power simulations, this model determines both steady and transient temperature fields in 3D multi-layer chip stacks with pin-fin-enhanced micro-gaps. Liquid cooling under spatially and temporally varying heat-flux distributions

has been studied under forced convection single-phase flow (Chapter 5). Passive liquid cooling capacities for each layer of 3D-SICs have also been experimentally studied in a thermosyphon loop with dielectric coolant Novec 7200. Characteristics of thermosyphon cooling approach have been studied for evaluation of cooling performance. Non-uniform cooling capacities for each layer of 3D-SIC evaporator have been found (Chapter 6).

7.1 Conclusions

The conclusions of this thesis will be presented for: active single-phase liquid cooling, and passive two-phase liquid cooling.

7.1.1 Active Single-Phase Cooling Approach

Non-uniform pin-fin structures (cylindrical pins and hydrofoil fins) contribute distinctly to single-phase liquid cooling performance: hydrofoil fins with increased fin density along the entire span have better cooling performance, because of the larger contact surface, but at a higher pressure drop. This enhanced cooling performance cannot be achieved by locally increased fin density only around the hotspot area, as the local higher flow resistance leads to a lower flow rate as well as cooling performance. On the contrary, cylindrical pins with smaller flow contact surface area and flow resistance do not require increased density all along the spanwise direction. Locally enhanced pin density only around the hotspot provides similar cooling capacity and pressure drop. Although both non-uniform cylindrical pin designs have a lower pressure drop, neither achieves the cooling performance of the spanwise increased hydrofoil fin design. It is suggested to place hotspot components with enhanced hydrofoil fin density along the spanwise direction to achieve better hotspot thermal management. For the pumping power sensitive or lower

cooling capacity requirement scenario, cylindrical pins can be adopted and these enhanced pin densities can be placed only above the local hotspot areas, which can enable more flexibility of hotspot arrangements.

To achieve improved cooling capacity with lower pumping power, hybrid heterogeneous pin and fin structures have been investigated in a single-phase liquid cooling manifold with 2.5D-SICs. Specially designed “Bridge-wing” flow guiding structures centred the flow for the high heat flux dies, and straight fins above the structure contributed to enhanced cooling performance of the upstream dies. Although these straight fins suffer from higher pressure drop, they have better cooling performance compared to cylindrical pins, as straight fins also serve a flow guiding function, to ensure higher flow rate over the high heat flux dies. For the lower heat flux dies downstream, cylindrical pins as cooling enhancement structures are adopted to have lower pressure drop to meet pumping power requirements.

When using a dielectric coolant, direct chip level liquid cooling can be achieved in the cooling manifold and the space between dies filled with the coolant. With active single-phase liquid cooling, the pumped coolant in this narrow space can remove the heat from two neighbour dies by forced convection. Thus, thermal isolation between heterogeneous chips in 2.5D-SICs can be achieved with this narrow coolant filled space (1 mm). This finding provides a thermal isolation approach for the heterogeneous die arrangement process in the design of such architectures. It is worth noting that this finding is not limited to achieve thermal isolation only between two heterogeneous dies. In fact, it can be adopted to solve thermal coupling issues in the future multiple die system and ensure functionalities of 2.5D-SICs.

For single-phase liquid cooling of avionics components, PAO (Polyalphaolefin) has superior thermal properties among various engineered fluids. However, it has higher pumping power consumption because of higher viscosity. Overall, this stable PAO coolant can be used for most of the working conditions, even at inlet temperature of 55 °C in simulated scenarios. The required pumping power is still lower than 0.5 W in the designed manifold for a total heat removal rate of 170 W. It is worth noting that the cooling performance of PAO is inferior to water under similar conditions.

Outlet location and size significantly impact the thermal and hydraulic performance of the cooling manifold. To achieve best cooling performance, smaller outlet area located on top of the center die contributed to extended flow path and uniform cooling capacity for the die. Multiple outlets should be avoided in multiple dies system, as the majority of coolant would directly flow to the outlets with shorter flow path on the dies, which could contribute to hotspots in the system. Guiding fins that did not confine along the entire spanwise direction did not lead to an extended flow path to alleviate hotspots. Overall, a carefully designed single-phase liquid cooling manifold, with heterogeneous pin-fin enhancement flow guiding structures can provide enhanced cooling capacity to compensate for the limitations of dielectric thermal properties, and overcome the thermal challenge of 2.5D-SICs with high heat flux components.

As we can assert from these mentioned findings that multiple heterogeneous dies would require multiple individually optimized heterogeneous pin-fin structures. These heterogeneous liquid cooling enhancement structures would interact with each other from both thermal and hydraulic perspectives as these are in the same fluidic system, located upstream to downstream. Systematical optimization of all the cooling enhancement

structures needs to be performed to deduce the interaction effects between these dies and ensure optimized cooling for the multidie structure. DoE method, coupled with CFD/HT, can achieve this objective by considering all the selected characteristic configurations of heterogeneous pin-fin structures. The evaluation process of DoE depends on matrix manipulations and the physical simulation results from CFD/HT. This optimization approach could ensure the optimality of the selected configuration, without a trial and error approach. This cost-effective approach does not have a limitation on the number of components and their configurations, and can be further applied to multiple components with multiple configurations for both 2.5D and 3D-SICs. Thus, the DoE method in conjunction with CFD/HT full scale simulations is a cost-effective, systematic thermal management optimization approach for both 2.5D and 3D-SICs, with heterogeneous cooling enhancement structures.

In addition to the optimization approach for cooling enhancement structures, a rapid thermal-electrical co-design simulation approach has been investigated for liquid cooling of 3D-SIC with TSVs. This approach considers convection heat transfer between coolant and pin-fins in the micro-gaps, heat conduction between stacked layers through TSVs, coupling with electrical co-design features to deduce leakage power under both steady state and transient realistic conditions. Dynamic power map in each layer can be implemented in this co-design model, enabling a rapid thermal-electrical simulation approach. Thermal simulation challenge of heterogeneous dies with time and location varying power maps, such as programmed FPGA with transient and moving hotspots can be handled. It is worth noting that when power of certain dies in the heterogeneous 3D-SIC system are relatively constant and high, it is suggested to locate these high heat flux dies in the upstream coolant

for each micro-gap layer to alleviate hotspots. This thermal-electrical simulation approach also contributes to better thermal management investigation of 3D-SIC manifold/package design, including coolant supply and removal, for each micro-gap.

7.1.2 Passive Two-Phase Liquid Cooling Approach

The first experimental implementation of miniature-thermosyphon with the evaporator consisting of stacked heaters with micro-gaps proves the feasibility and provides the preliminary cooling capacity of passive two-phase liquid cooling for 3D-SICs.

Riser height difference between evaporator and condenser plays an important role on thermosyphon 3D-SIC cooling. Compared to riser height of 28 cm, riser height of 56 cm provided increased cooling capacity, as high as 5 W/cm^2. This cooling capacity can be further increased with higher riser height. Riser height of 56 cm can be easily achieved in a data center rack by placing the condenser at the top of the rack. It is also worth noting that, 3D-SIC evaporators at 0^o tilting angle, which performed well, would be thin enough to be placed in a 1U server. Thus, multiple 3D-SICs can be placed inside of various 1U servers of with condenser on the top of that rack. 3D-SICs with higher power can be placed on the lower level 1U servers to achieve enhanced cooling performance because of increased riser height. Cooling capacity of these thermosyphon can be controlled by adjusting the condenser inlet chilled-water temperature. The lower the chilled water temperature at inlet of condenser, the better cooling performance of thermosyphon for 3D-SICs. It is worth noting that, for each 3D-SIC evaporator, cooling capacities decrease from the top chip layer to the bottom chip layer. Within each layer, cooling capacities decrease from upstream to downstream. These non-uniform cooling capacities in each 3D-SIC

evaporator should be taken into consideration for 3D-SIC die arrangements. In short, thermosyphon two-phase liquid cooling approach, which provides non-uniform in-plane as well as cross-plane cooling capacities for multi-layer evaporator, can be used for 3D-SICs with heterogeneous chips. This approach is feasible for data center 3D-SIC pump-free liquid cooling application and can achieve further enhanced cooling capacities in various server configerations.

7.2 Recommendations for Future Work

7.2.1 Active Liquid Cooling

Non-uniform pin-fin structures can be extended to more complicated 2.5D and 3D-SIC configurations, which could lead to different flow fields and additional thermal management challenges. In addition to cooling enhancement of non-uniform pin-fin structures with single-phase liquid cooling, compact co-design simulation tool can be further extended to rapid two-phase transient cooling simulations with electrical co-design to achieve efficient and realistic simulations without relying on the resource consuming full field CFD/HT method.

7.2.2 Passive Liquid Cooling

Although the thermosyphon loop including 3D evaporator as 3D-SICs has been designed, built and experimentally tested under various loop configurations to determine the passive two-phase cooling capacities for each layer of 3D-SICs, the cooling performance can be further enhanced. In the 3D-SIC evaporator, fundamental studies of bubble location and frequency, and flow regimes in the micro-gaps between chips could

contribute to better understanding of the multi-layer chip temperatures and bubble dynamics as well as dry out conditions. Flow distributions for each micro-gap at the inlet of evaporator relate to the boiling phenomena in each layer and are yet to be studied. Additionally, vapor generated from various micro-gaps collecting at the outlet of evaporator could affect cooling performance of each layer of 3D-SICs. This vapor collection phenomenon is related to the evaporator channel design and is worthy of investigation, as the thermosyphon driving force due to buoyancy force is critical to the cooling performance.

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